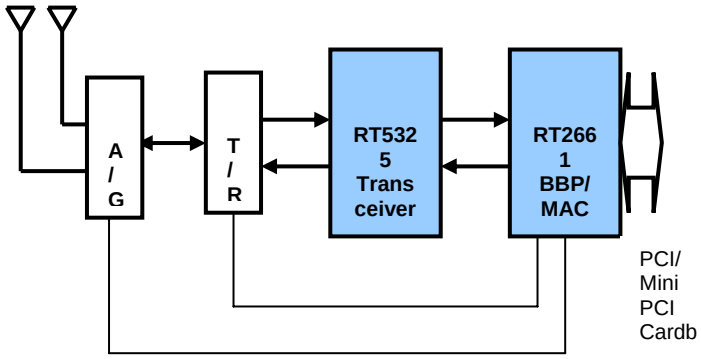
Applications

- IEEE 802.11 a/b/g Wireless Local Area Networks
- Wireless Media Adaptors/Wireless Video Streaming
- Wireless Portable Devices/Notebook Computers
- Smart antenna wireless system

RT2661 is the MAC/BBP IC for Ralink RT2600 chipset. RT2600 is Ralink 802.11a/b/g **SMART** G™ or **SMART** AG™ chipset and consists of two highly integrated ICs (RT5325 and RT2661) that fully comply with IEEE 802.11a/b/g standard. The chipset achieves robust high throughput from a long distance supported with all the features improvement from Ralink proven 802.11a/b/g technology. Optimized two chips RF and BBP/MAC smart antenna solution provides superb performance with competitive cost, which also provides an excellent choice 802.11 a/b/g and b/g other than traditional solutions. Intelligent MAC design deploys high efficient DMA engine and AES/WEP security engine without overloading host processor. The RT2600 is designed to support standard based features in the areas of security, quality of service and international regulation, giving end users greatest performance anytime in any circumstance.

Functional Block Diagram



Features

- CardBus / Mini PCI / PCI Interface
- PCI 2.2 compliant
- Bus Master Design for Low CPU Utilization
- Security – WEP 64/128, TKIP, WPA, WPA2, 802.11i
- Quality of Service (QOS) - 802.11e, WMM
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- 6, 9, 12, 18, 24, 36, 48, 54 Mbps for OFDM; 5.5, 11Mbps for CCK; and 1, 2Mbps for Barker Modulation.
- Packet-OVERDRIVE ™ Technology
- Range-OVERDRIVE ™ Technology
- Bluetooth Co-existence
- Low Power with Advanced Power Management
- Serial EEPROM, LEDs, GPIOs Interface
- Operating Systems - Windows XP, 2000, ME, 98SE, Linux, MAC
- 14 mm x 14 mm EPAD-TQFP-128 Package
- 3.3V/1.8V, 3/5V PCI I/O

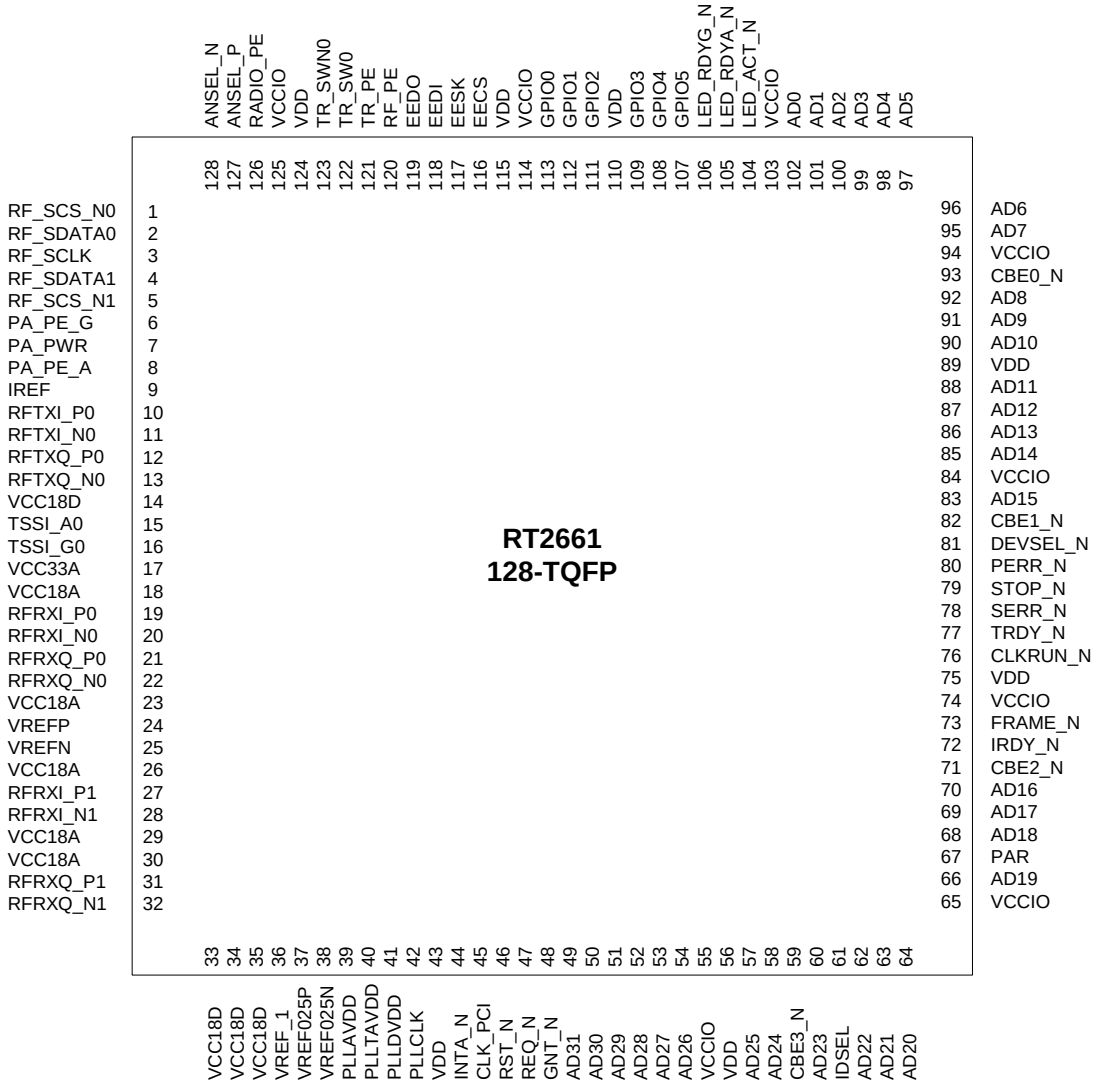
Order Information

Part Number	Temp Range	Package
RT2661T	-10 to 85°C	Lead-free 128L E-PAD TQFP

Ralink Technology, Corp. (Taiwan)
4th Fl. No. 2, Technology 5th Rd. SBIP
Hsin-Chu,Taiwan, R.O.C.
Tel: 886-3-567-8868
Fax: 886-3-567-8818

Ralink Technology, Corp. (USA)
20833 Stevens Creek Blvd.
Ste 200 Cupertino, CA95014
Tel: (408) 725-8070
Fax:(408)725-8069
http://www.ralinktech.com

Pin Assignment



Pin Description

Pin	Name	Type	Description
Analog controlled RF interface: 41 pins			
1	RF_SCS_N0	O	RF channel 0 RPI interface selection, active low
2	RF_SDATA0	O	RF channel 0 RPI interface data.
3	RF_SCLK	O	RF RPI interface clock for all RF channels
4	RF_SDATA1	O	RF channel 1 RPI interface data.
5	RF_SCS_N1	O	RF channel 1 RPI interface selection, active low
6	PA_PE_G	O	LDO output for G band RF power amplifier enable control
7	PA_PWR	P	Power supply of PA_PE LDO
8	PA_PE_A	O	LDO output for A band RF power amplifier enable control
9	IREF	I	Reference current input to ADC/DAC
10	RFTXI_P0	O	Positive signal of TX I differential output from 10bit DAC
11	RFTXI_N0	O	Negative signal of TX I differential output from 10bit DAC
12	RFTXQ_P0	O	Positive signal of TX Q differential output from 10bit DAC
13	RFTXQ_N0	O	Negative signal of TX Q differential output from 10bit DAC
15	TSSI_A0	I	Single end A band TSSI signal input to 5bit ADC
16	TSSI_G0	I	Single end G band TSSI signal input to 5bit ADC
19	RFRXI_P0	I	Positive signal of RX I differential input to 8bit ADC0
20	RFRXI_N0	I	Negative signal of RX I differential input to 8bit ADC0
21	RFRXQ_P0	I	Positive signal of RX Q differential input to 8bit ADC0
22	RFRXQ_N0	I	Negative signal of RX Q differential input to 8bit ADC0
24	VREFP	O	Reference voltage output point P for external bypass cap
25	VREFN	O	Reference voltage output point N for external bypass cap
27	RFRXI_P1	I	Positive signal of RX I differential input to 8bit ADC1
28	RFRXI_N1	I	Negative signal of RX I differential input to 8bit ADC1
31	RFRXQ_P1	I	Positive signal of RX Q differential input to 8bit ADC1
32	RFRXQ_N1	I	Negative signal of RX Q differential input to 8bit ADC1
36	VREF	O	Reference voltage output for external bypass cap
37	VREF025P	O	Reference voltage output point ¼ P for external bypass cap
38	VREF025N	O	Reference voltage output point ¼ N for external bypass cap
17	VCC33A	P	3.3V analog power supply
18,23,26,29, 30	VCC18A	P	1.8V analog power supply
14,33,34,35	VCC18D	P	1.8V digital power supply to ADC/DAC should be

Pin	Name	Type	Description
			isolated from power supply VDD for digital core
39	PLLAVDD	P	1.8V analog power supply to PLL
40	PLLTAVDD	P	1.8V analog power supply to PLL
41	PLLDVDD	P	1.8V digital power supply to PLL
Digital controlled RF interface: 7 pins			
120	RF_PE	O	RX and TX enable control for RF transceiver.
121	TR_PE	O	RX and TX enable control for RF transceiver.
122	TR_SW0	O	Positive signal of RX and TX switching control
123	TR_SWN0	O	Negative signal of RX and TX switching control
126	RADIO_PE	O	Radio power off
127	ANSEL_P	O	Positive signal of antenna selection
128	ANSEL_N	O	Negative signal of antenna selection
PCI: 52 pins			
42	PLLCLK	I	40MHz clock for internal PLL.
44	INTA_N	O	PCI interrupt
45	CLK_PCI	I	PCI clock
46	RST_N	I	PCI reset
47	REQ_N	O	PCI bus request
48	GNT_N	I	PCI bus granted
49	AD31	I/O	PCI address and data
50	AD30	I/O	PCI address and data
51	AD29	I/O	PCI address and data
52	AD28	I/O	PCI address and data
53	AD27	I/O	PCI address and data
54	AD26	I/O	PCI address and data
57	AD25	I/O	PCI address and data
58	AD24	I/O	PCI address and data
59	CBE3_N	I/O	PCI bus command and byte enable
60	AD23	I/O	PCI address and data
61	IDSEL	I	PCI initialization device select
62	AD22	I/O	PCI address and data
63	AD21	I/O	PCI address and data
64	AD20	I/O	PCI address and data
66	AD19	I/O	PCI address and data
67	PAR	I/O	PCI parity
68	AD18	I/O	PCI address and data
69	AD17	I/O	PCI address and data
70	AD16	I/O	PCI address and data
71	CBE2_N	I/O	PCI bus command and byte enable
72	IRDY_N	I/O	PCI initiator ready
73	FRAME_N	I/O	PCI cycle frame
76	CLKRUN_N	I/O	PCI clock running
77	TRDY_N	I/O	PCI target ready
78	SERR_N	O	PCI system error
79	STOP_N	I/O	PCI target stop
80	PERR_N	I/O	PCI parity error
81	DEVSEL_N	I/O	PCI device select
82	CBE1_N	I/O	PCI bus command and byte enable
83	AD15	I/O	PCI address and data
85	AD14	I/O	PCI address and data
86	AD13	I/O	PCI address and data
87	AD12	I/O	PCI address and data

Pin	Name	Type	Description
88	AD11	I/O	PCI address and data
90	AD10	I/O	PCI address and data
91	AD9	I/O	PCI address and data
92	AD8	I/O	PCI address and data
93	CBE0_N	I/O	PCI bus command and byte enable
95	AD7	I/O	PCI address and data
96	AD6	I/O	PCI address and data
97	AD5	I/O	PCI address and data
98	AD4	I/O	PCI address and data
99	AD3	I/O	PCI address and data
100	AD2	I/O	PCI address and data
101	AD1	I/O	PCI address and data
102	AD0	I/O	PCI address and data
LED: 3 pins			
104	LED_ACT_N	O	LED flash in transmission
105	LED_RDYA_N	O	LED active while operation in A mode.
106	LED_RDYG_N	O	LED active while operation in G mode.
GPIO: 6 pins			
107	GPIO5	I/O	GPIO. Also used as radio status monitor.
108	GPIO4	I/O	GPIO
109	GPIO3	I/O	GPIO
111	GPIO2	I/O	GPIO
112	GPIO1	I/O	GPIO
113	GPIO0	I/O	GPIO
EEPROM: 4 pins			
116	EECS	O	serial EEPROM chip select
117	EESK	O	serial EEPROM clock
118	EEDI	O	serial output to EEPROM
119	EEDO	I	serial input from EEPROM
Digital Power: 15 pins			
55,65,74,84, 94,103,114,125	VCCIO	P	3.3V digital power supply
43,56,75,89, 110,115,124	VDD	P	1.8V digital power supply
Total: 128 pins			

Absolute Maximum Ratings

Core Supply Voltage 1.98V
I/O Supply Voltage 3.6V
Input, Output or I/O Voltage.. . . . . GND –0.3V to Vcc+0.3V

Thermal Information

Thermal Resistance θ_{JA} (^{o}C/W) in free air for E-PAD TQFP (14x14mm) package.. . . . . .24.1 ^{o}C/W
Maximum Junction Temperature . . . . . .125^{o}C
Maximum Storage Temperature . . . . . -40^{o}C to 150^{o}C

Operating Conditions

Ambient Temperature Range . . . . . -10 to 85^{o}C
Core Supply Voltage . . . . . 1.8V +/- 10%
I/O Supply Voltage . . . . . 3.3V +/- 10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

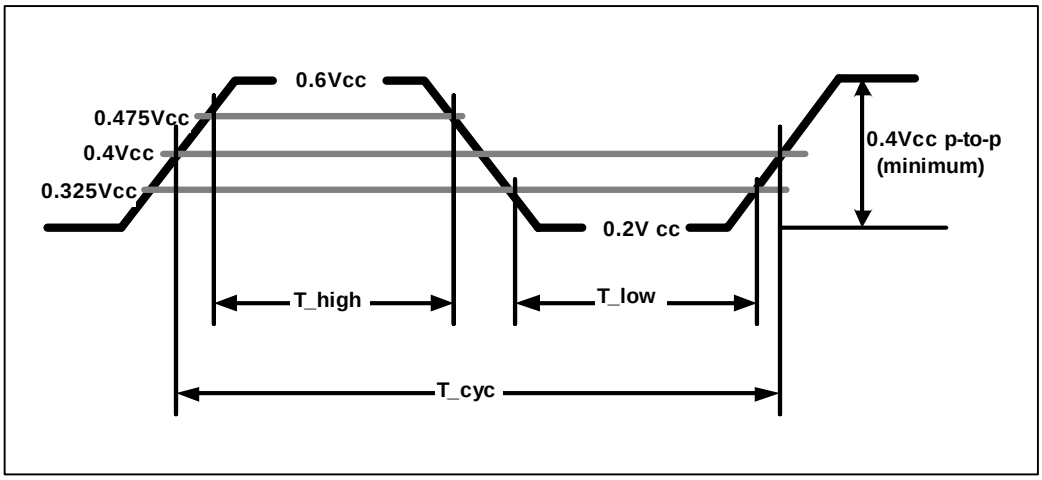
DC Electrical Specifications

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Power supply current(*Note1)	I_{CCOP}	V_{DD} = Max, frequency 33 & 44MHz		170		mA
Standby power supply current	I_{CCSB}	V_{DD} = Max, output not loaded		25		mA
Input leakage current	I_I	V_{DD} = Max, input = 0 or V_{DD}			10	μA
Tri-state output leakage current	I_{OZ}	V_{DD} = Max, input = 0 or V_{DD}			10	μA
Logical one input voltage	V_{IH}		2.0		5.5	V
Logical zero input voltage	V_{IL}		-0.3		0.8	V
Logical one output voltage	V_{OH}	I_{OH} = -1mA, V_{DD} = Min	2.4			V
Logical zero output voltage	V_{OL}	I_{OL} = 2mA, V_{DD} = Min			0.4	V
Input capacitance	C_{IN}	CLKIN frequency 1MHz. All measurements referenced to GND. T_A = 25 ^{o}C		4.0		pF

**Note1: whole chip current measured on 3.3V power, 1.8V power is combined to 3.3V through LDO regulator.*

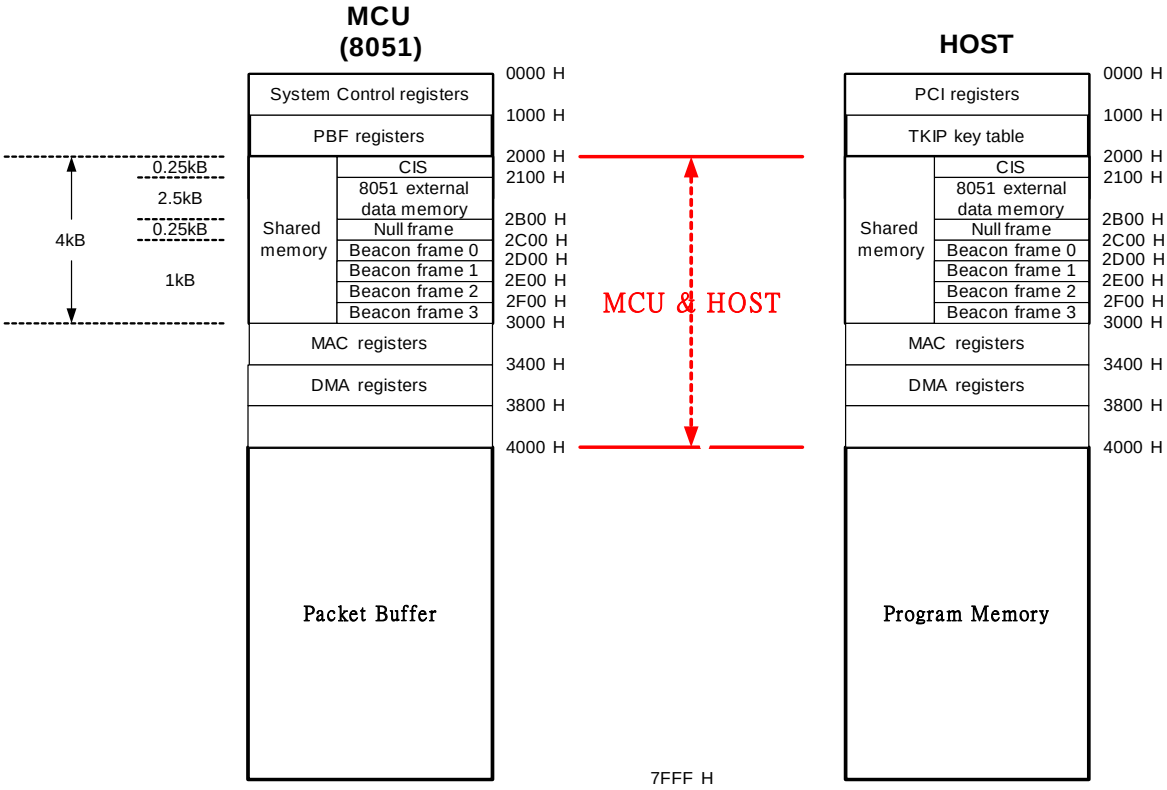
AC Electrical Specifications

CardBus / MiniPCI / PCI Clock Specification



Symbol	Parameter	Min	Max	Units	Notes
T_{cyc}	CLK Cycle Time	30		ns	
T_{high}	CLK High Time	11		ns	
T_{low}	CLK Low Time	11		ns	
T_{slew}	CLK Slew Rate	1	4	V/ns	

Register map



MAC_CORE Register (Base Address = 0x3000)

MAC Control Register

W/R: writable and readable
RO: read-only
WO: write only
RC: read-then-clear
WC: write-then-clear

MAC_CSR0: ASIC version number (offset = 3000h)

Field	Type	Default	Description
Bit 31:0	RO	0x2661a	MAC ASIC version number

MAC_CSR1: System control register (offset = 3004h)

Field	Type	Default	Description
Bit 31:3	RO	0x0	Reserved
Bit 2	R/W	0x0	Host is ready to work 1 = Ready
Bit 1	R/W	0x1	Hardware Reset BBP: 1: reset BBP 0: release reset
Bit 0	R/W	0x0	Soft-reset MAC 1 = MAC in reset state 0 = MAC in normal state This won't reset MAC register values.

MAC_CSR2: MAC address register 0 (offset = 3008h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	STA MAC address byte3
Bit 23:16	R/W	0x0	STA MAC address byte2
Bit 15:8	R/W	0x0	STA MAC address byte1
Bit 7:0	R/W	0x0	STA MAC address byte0 *Note: **byte0** is the first byte on network; its LSB is the first bit on network. For a MAC address captured on the network 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_CSR3: MAC address register 1 (offset = 300Ch)

Field	Type	Default	Description
Bit 31:24	RO	0x0	Reserved
Bit 23:16	R/W	0xFF	"Unicast-to-me" comparison mask for received Address1 and MAC Address on byte5 0: don't care 1: compare
Bit 15:8	R/W	0x0	STA MAC address byte5
Bit 7:0	R/W	0x0	STA MAC address byte4

- The multiple BSSID mask for byte5 in MAC_CSR5 also takes effect on unicast-to-me comparison. The "final" unicast-to-me compare mask on byte5 is (uc_to_me_mask[7:0] & bssid_mask[1:0]).

MAC_CSR4: BSSID register 0 (offset = 3010h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	BSSID byte3
Bit 23:16	R/W	0x0	BSSID byte2
Bit 15:8	R/W	0x0	BSSID byte1
Bit 7:0	R/W	0x0	BSSID byte0

MAC_CSR5: BSSID register 1 (offset = 3014h)

Field	Type	Default	Description
Bit 31:18	RO	0x0	Reserved
Bit 17:16	R/W	0x3	Multiple BSSID comparison mask, 0: don't care, 1: enable Bit16: comparison mask bit0 of BSSID byte6(MAC_CSR5 bit8) Bit17: comparison mask bit1 of BSSID byte6(MAC_CSR5 bit9) The value will also affect the number of shared keys in the key table. 11: one BSSID; 01, 10: two BSSID; 00: four BSSID
Bit 15:8	R/W	0x0	BSSID byte5
Bit 7:0	R/W	0x0	BSSID byte4

- The multiple BSSID mask is used to make bit0, bit1 of BSSID byte5 "don't care" in RX BSSID comparison (which result in "is_my_bssid" flag in RX descriptor).

MAC_CSR6: Maximum frame length register (offset = 3018h)

Field	Type	Default	Description
Bit 31:12	RO	0x0	Reserved
Bit 11:0	R/W	0x780	Maximum Frame length in byte unit Default value is1920 bytes, i.e. (128Byte * 16)

- ASIC will block incoming frames longer than this maximum size to prevent overwriting RX buffer.

MAC_CSR7: Reserved (offset = 301Ch)

Field	Type	Default	Description
Bit 31: 0	RO	0x0	Reserved

MAC_CSR8: SIFS / EIFS register (offset = 3020h)

Field	Type	Default	Description
Bit 31:16	R/W	0x16C	EIFS in unit of 1-us Default 364 us
Bit 15:8	R/W	0x00	SIFS in unit of 1-us, applied after OFDM RX to compensate OFDM RX PHY delay
Bit 7:0	R/W	0x0A	SIFS in unit of 1-us, applied after CCK TX/RX and OFDM TX Default 10 us for 11b/g. Driver will change it to 16 us when operating in 11a

MAC_CSR9: Slot time / contention window register (offset = 3024h)

Field	Type	Default	Description
Bit 31:17	RO	0x0	Reserved
Bit 16	R/W	0x0	Use following default value as {cwmin, cwmax} pair. Ignore the {cwmin, cwmax} pair in TX descriptor.
Bit 15:12	R/W	0xa	Defaul value of cwmax
Bit 11:8	R/W	0x3	Default value of cwmin
Bit 7:0	R/W	0x14	Slot time in unit of 1-us. This value is used by Backoff engine to calculate the total backoff time. Default 20us for 11b/g. 11a and 11g-short-slot-mode is 9 us

MAC_CSR10: Power mode configuration register (offset = 3028h)

Field	Type	Default	Description
Bit 31:13	RO	0x0	Reserved
Bit 12	R/W	0x0	BBP AD/DA power down in Awake state
Bit 11	R/W	0x0	BBP PLL power down in Awake state
Bit 10	R/W	0x1	RA_PE in Awake state
Bit 9	R/W	0x1	RF_PE in Awake state
Bit 8	R/W	0x1	TR_PE in Awake state (change to 0 automatically when TX)
Bit 7:5	RO	0x0	Reserved
Bit 4	R/W	0x1	BBP AD/DA power down in Sleep state
Bit 3	R/W	0x1	BBP PLL power down in Sleep state
Bit 2	R/W	0x0	RA_PE in Sleep state
Bit 1	R/W	0x0	RF_PE in Sleep state
Bit 0	R/W	0x0	TR_PE in Sleep state

MAC_CSR11: Power saving transition time register (offset = 302Ch)

Field	Type	Default	Description
Bit 31:20	RO	0x0	Reserved
Bit 19:16	R/W	0xA	Transition time from Sleep to Awake in units of 1-TU (1.024ms) Default: 10 state transition from awake to sleep is 0 by default but will postpone until TX and RX process became idle.
Bit 15	R/W	0x0	Enable Auto Wakeup timer interrupt

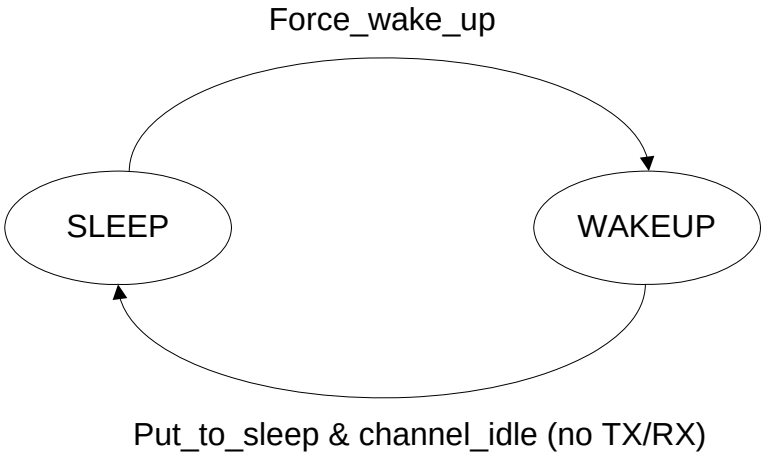
			Once enabled, ASIC will auto wakes up BBP/RF to AWAKE state after the specified time (TbcnExp# * BeaconInterval + DelayAfterLastTbcnExp) has past.
Bit 14:8	R/W	0x0	Number of subsequent Tbcn Expirations before Wakeup Default: 0
Bit 7:0	R/W	0x50	Delay after the last Tbcn expiration in unit of 1-TU Default is 80, which means 20 TU ahead of next TBTT. This lead time should be sufficient for BBP/RF to recover from whatever power state to AWAKE state

- CAUTION!! Please make sure TBTT timer is enabled if auto wakeup interrupt timer is enabled.

MAC_CSR12: Power state control register (offset = 3030h)

Field	Type	Default	Description
Bit 31:4	RO	0x0	Reserved
Bit 3	RO	0x0	0: BB/RF is not ready 1: BB/RF is stable
Bit 2	WC	0x0	Force wake up, write 1 to put BBP/RF to AWAKE state.
Bit 1	WC	0x0	Put to sleep, write 1 to put BBP/RF to SLEEP state.
Bit 0	RO	0x0	Power state, 0:SLEEP mode, 1: AWAKE state

- "Put to sleep" command may not be execute right away due to channel busy. The command postpone time is random.
- "Force wake up" command will cancel the "Put to sleep" command and wake up MAC immediately anyhow.
- CAUTION!! If "Put to sleep" command is issued but power state does not go to sleep state after a long time(due to random postpone time), please issue "Force wake up" command to cancel "Put to sleep" command before treat MAC as in AWAKE state.
- "Force wake up" command has higher priority than "Put to sleep" command if they are issued at the same time.



MAC_CSR13: GPIO control register (offset = 3034h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:14	R/W	0x3	Reserved.
Bit 13:8	R/W	0x3F	GPIO5-0 direction, 0:output, 1: input
Bit 7:6	R/W	0x00	Reserved.
Bit 5:0	R/W	0x00	GPIO5-0 value

MAC_CSR14: LED control register (offset = 3038h)

Field	Type	Default	Description
Bit 31:20	RO	0x0	Reserved
Bit 19	R/W	0x0	Software controlled LED_RDYG_A LED 1: ON, 0:OFF
Bit 18	R/W	0x0	ASIC controlled TX activity LED polarity 0: Low active 1: High active
Bit 17	R/W	0x0	Software controlled LED_RDYG_N LED 1: ON, 0:OFF
Bit 16	R/W	0x0	ASIC controlled TX activity LED 1: Enable, blinking upon TX 0: Disable
Bit 15:8	R/W	0x1E	Off period in unit of 1-ms Default: 30ms
Bit 7:0	R/W	0x46	On period in unit of 1-ms Default: 70ms

MAC_CSR15: NAV control register (offset = 303Ch)

Field	Type	Default	Description
Bit 31:16	RO	0x0	MAC NAV current counter value (count down, unit: 1us)
Bit 15	WC	0x0	1: Update MAC NAV down-counter value
Bit 14:0	R/W	0x0	New NAV value for update (unit: 1us)

TXRX Control Register

TXRX_CSR0: TX/RX configuration register (offset = 3040h)

Field	Type	Default	Description
Bit 31:26	RO	0x0	Reserved
Bit 25	R/W	0x0	Drop ACK/CTS frame
Bit 24	R/W	0x0	Drop broadcast frame
Bit 23	R/W	0x0	Drop multicast frame
Bit 22	R/W	0x1	Drop version error frame
Bit 21	R/W	0x1	Drop ToDs frame 1 = drop all frames with ToDs bit on
Bit 20	R/W	0x1	Drop not to me unicast frame 1 = do not pass unicast-but-not-to-me frames to host
Bit 19	R/W	0x1	Drop control frame
Bit 18	R/W	0x1	Drop physical error frame
Bit 17	R/W	0x1	Drop CRC error frame
Bit 16	R/W	0x1	Disable RX
Bit 15	R/W	0x1	ASIC maintains TX frame's SEQ# 1: enable this feature 0: disable. Let software maintains seq#.
Bit 14:9	R/W	0x18	TSF offset in MAC header Default value is 24. For outgoing frames, if InsertTsf falg in ON in TX descriptor (for BEACON, ProbeResponse only), ASIC will overwrite the TSF field in the outgoing frame with the local TSF. For incoming BEACON frame, ASIC extract remote TSF at this offset and perform TSF synchronization.
Bit 8:0	R/W	0x32	RX ACK Timeout in unit of 1-us Default value is 50us. If CCA is not asserted within this time limit, ASIC will retry the transmission.

TXRX_CSR1: RX descriptor BBP ID register (offset = 3044h)

Field	Type	Default	Description
Bit 31	R/W	0x1	BBP register 1 Valid
Bit 30:24	R/W	0x33	BBP register 1 ID, default is R51 OFDM RSSI
Bit 23	R/W	0x1	BBP register 0 Valid
Bit 22:16	R/W	0x2A	BBP register 0 ID, default is R42 OFDM RATE
Bit 15	R/W	0x1	BBP register 1 Valid for CCK
Bit 14:8	R/W	0x33	BBP register 1 ID, default is R51 CCK RSSI
Bit 7	R/W	0x1	BBP register 0 Valid for CCK
Bit 6:0	R/W	0x2F	BBP register 0 ID, default is R47 CCK RATE

- The specified BBP register values will be automatically attached to the RX descriptor of every received frame

TXRX_CSR2: CCK TX descriptor BBP ID register (offset = 3048h)

Field	Type	Default	Description
Bit 31:24	R/W	0x8A	CCK SIGNAL register ID, default is R10
Bit 23:16	R/W	0x8B	CCK SERVICE register ID, default is R11
Bit 15:8	R/W	0x8C	CCK LENGTH_HIGH register ID, default is R12
Bit 7:0	R/W	0x8D	CCK LENGTH_LOW register ID, default is R13

TXRX_CSR3: OFDM TX descriptor BBP ID register (offset = 304Ch)

Field	Type	Default	Description
Bit 31:24	R/W	0x00	TX Power register ID
Bit 23:16	R/W	0x85	OFDM RATE register ID, default is R5
Bit 15:8	R/W	0x86	OFDM LENGTH_HIGH register ID, default is R6
Bit 7:0	R/W	0x87	OFDM LENGTH_LOW register ID, default is R7

TXRX_CSR4: Auto Responder / TX retransmission register (offset = 3050h)

Field	Type	Default	Description
Bit 31:28	R/W	0x7	Short retry limit, applied when TX descriptor -> retry_mode = 0
Bit 27:24	R/W	0x4	Long retry limit, applied when TX descriptor -> retry_mode = 1
Bit 23	R/W	0x0	1: Auto downgrade initial TX rate (ex:54 ->48) when consecutive retried TX result occurred, downgrade action is cancelled when consecutive no-retried TX result occurred. 0: disable
Bit 22	R/W	0x0	0: OFDM TX rate auto fallback to OFDM 6M only 1: OFDM TX rate auto fallback to CCK 1M, 2M
Bit 21:20	R/W	0x0	OFDM TX rate auto fallback speed 0: fallback one step in rate when TX retry 1: fallback two step in rate when TX retry 2: fallback three step in rate when TX retry 3: fallback four step in rate when TX retry (TX retry rate will not fallback below 6Mbps)
Bit 19	R/W	0x1	OFDM TX rate auto fallback enable
Bit 18	R/W	0x0	Auto responder CCK 2, 5.5, 11Mbps preamble selection 0: long preamble 1: short preamble (ACK/CTS auto responding in CCK 1Mbps always use long preamble.)
Bit 17	R/W	0x1	Enable auto responder 1 = enable ACK/CTS auto responder
Bit 16	R/W	0x0	ACK/CTS power-management bit in MAC header 1: STA in power-saving mode 0: STA in active mode
Bit 15:11	RO	0x0	Reserved
Bit 10:8	R/W	0x7	Auto responder ACK policy upon reception of following CONTROL frame, 0:disable 1:enable Bit8: For Block Acknowledgement Request (BlockAckReq) Bit9: For Block Acknowledgement (BlockAck) Bit10: For Power Save Poll (PS-Poll)
Bit 7:0	R/W	0x32	TX ACK/CTS time-out in unit of 1-us. Default is 50 us. This value specifies how long the “Auto Responder” will wait if an outgoing ACK/CTS is pending due to PHY busy. If an ACK/CTS can’t be sent within this period, it’ll be given up. Time-out timer will be clear once ACT/CTS TX is kicked.

- Upon reception unicast-to-me packet:
  1. For management frame, ACK is always replied in SIFS time.
  2. For data frame, ACK is replied in SIFS time according to FC.Qos bit and ACK policy (if Qos control field exists).
  3. For control frame (Block ACK Req, BlockACK, PS-Poll), ACK is replied in SIFS time according to TXRX_CSR4, bit10-8.
  4. For control frame (RTS), CTS is always replied in SIFS time.
  5. For control frame (ACK/CTS/CF-End/CF-End-Ack), no responds.

TXRX_CSR5: Auto responder basic rate, TX power register (offset = 3054h)

Field	Type	Default	Description
Bit 31:28	R/W	0x3	Auto upgrade limit (unit: no-retried packet)
Bit 27:24	R/W	0x3	Auto downgrade limit (unit: retried packet)
Bit 23:16	R/W	0x6	Auto responder TX power
Bit 15:12	RO	0x0	Reserved
Bit 11:0	R/W	0x0	Basic rate bit mask, bit0=1: 1 Mbps is basic rate, bit1=1: 2 Mbps is basic rate, bit2=1: 5.5 Mbps is basic rate, bit3=1: 11 Mbps is basic rate, bit4=1: 6 Mbps is basic rate, bit5=1: 9 Mbps is basic rate bit6=1: 12 Mbps is basic rate, bit7=1: 18 Mbps is basic rate, bit8=1: 24 Mbps is basic rate, bit9=1: 36 Mbps is basic rate, bit10=1: 48 Mbps is basic rate, bit11=1: 54 Mbps is basic rate

TXRX_CSR6: ACK/CTS payload consume time (offset = 3058h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0A	ACK/CTS Payload consume time @11M (in unit of 1 us)
Bit 23:16	R/W	0x14	ACK/CTS payload consume time @5.5M (in unit of 1 us)
Bit 15:8	R/W	0x38	ACK/CTS Payload consume time @2M (in unit of 1 us)
Bit 7:0	R/W	0x70	ACK/CTS Payload consume time @1M (in unit of 1 us)

TXRX_CSR7: ACK/CTS payload consume time (offset = 305Ch)

Field	Type	Default	Description
Bit 31:24	R/W	0x06	ACK/CTS payload consume time @18M (in unit of 1-us)
Bit 23:16	R/W	0x09	ACK/CTS payload consume time @12M (in unit of 1-us)
Bit 15:8	R/W	0x0C	ACK/CTS payload consume time @9M (in unit of 1-us)
Bit 7:0	R/W	0x13	ACK/CTS payload consume time @6M (in unit of 1-us)

TXRX_CSR8: ACK/CTS payload consume time (offset = 3060h)

Field	Type	Default	Description
Bit 31:24	R/W	0x02	ACK/CTS payload consume time @54M (in unit of 1-us)
Bit 23:16	R/W	0x03	ACK/CTS payload consume time @48M (in unit of 1-us)
Bit 15:8	R/W	0x03	ACK/CTS payload consume time @36M (in unit of 1-us)
Bit 7:0	R/W	0x05	ACK/CTS payload consume time @24M (in unit of 1-us)

- ASIC utilizes these registers (TXRX_CSR6,7,8) together with the received unicast-to-me frame's "duration" field to decide the "duration" value in the outgoing ACK/CTS frame.

TXRX_CSR9: Beacon Synchronization register (offset = 3064h)

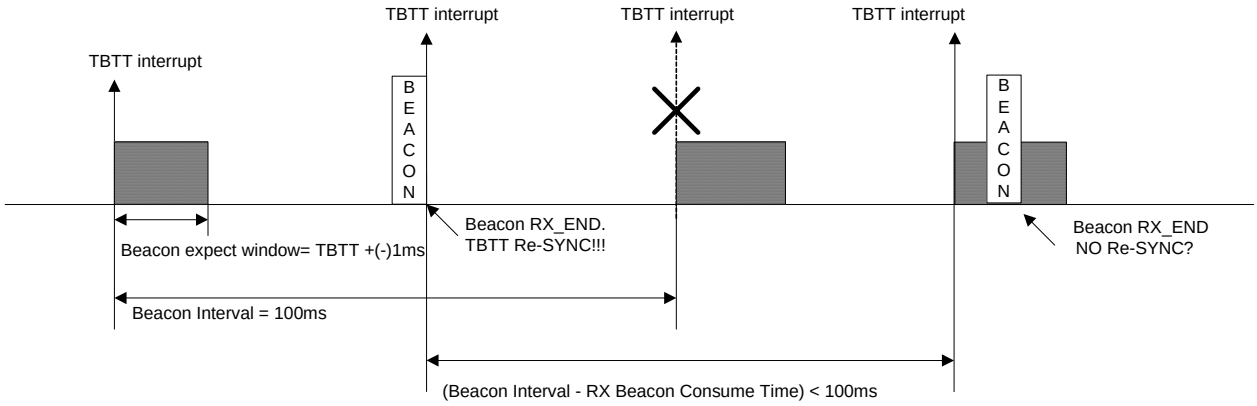
Field	Type	Default	Description
Bit 31:24	R/W	0x0	TX timestamp insertion compensation value, default: 0
Bit 23:21	RO	0x0	Reserved
Bit 20	R/W	0x0	Enable BEACON TX at TBTT interrupt
Bit 19	R/W	0x0	Enable TBTT timer. A "TBTT interrupt" will happen every "BEACON interval 0 = stop TBTT timer

			1 = start TBTT timer
Bit 18:17	R/W	0x0	Synchronize local TSF with remote TSF in the received BEACON frame. 00 = disable 01 = always sync with received “is_mybssid” BEACON (station infra-structure mode) 10 = sync with received “is_mybssid” BEACON only if the remote TSF is greater than local TSF (station ad hoc mode) 11 = sync with no body (AP mode)
Bit 16	R/W	0x0	Enable TSF 1 = start TSF auto counting 0 = stop TSF auto counting A 0-to-1 transition will cause TSF to re-start from 0.
Bit 15:0	R/W	0x0640	BEACON interval in unit of 1/16 TU (64us) Default value is 1600 (=100 TU = 102.4 ms) Maximum beacon interval is about 4000ms

TXRX_CSR10: Beacon time alignment register (offset = 3068h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:8	R/W	0x10	Beacon Expecting window (unit: 64us), default value is 64*16=1024us(that is, 1% of beacon interval) The window starts right after TBTT interrupt; TBTT timer will not synchronize its phase with remote STA upon receiving “is_my_bssid” beacon in this window.
Bit 7:0	R/W	0x10	IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us. In IBSS mode(Ad hoc), if consecutive TX beacon failures (or consecutive success)happened, TBTT timer will adjust it phase to meet will external TBTT time.

- Upon receiving a is_my_bssid BEACON from AP or remote peer “AND” RXEnd event is not in beacon expecting window, ASIC would re-align next TBTT to be (local TSF + Beacon interval – RX Beacon Consume Time).
- (RX Beacon Consume Time) is the time from CCA assertion to RXEND event of the beacon.



TXRX_CSR11: AES frame control AND/OR mask register (offset = 306Ch)

Field	Type	Default	Description
Bit 31:16	R/W	0x0000	Frame control field OR mask in AES encryption/decryption (applied after AES AND mask below)
Bit 15:0	R/W	0xc78F	Frame control field AND mask in AES encryption/decryption

TXRX_CSR12: MAC TSF Timer Low register (offset = 3070h)

Field	Type	Default	Description
Bit 31:0	RO	0x0000	MAC local 64-bit TSF timer value bit31-0

TXRX_CSR13: MAC TSF Timer High register (offset = 3074h)

Field	Type	Default	Description
Bit 31:0	RO	0x0000	MAC local 64-bit TSF timer value bit63-32

TXRX_CSR14: MAC TBTT Timer register (offset = 3078h)

Field	Type	Default	Description
Bit 31: 17	RO	0x0000	Reserved
Bit 16:0	RO	0x0000	TBTT Timer, which means time remains before next TBTT time, (unit: 32us) When TXRX_CSR9.bit19 TBTT timer is enabled, the value will down count from beacon interval value specified in TXRX_CSR9.bit15-0 to 0 in unit of 32us. The value of the timer is 0 when TBTT timer is disabled.

TXRX_CSR15: TKIP MIC Priority Byte AND Mask register (offset = 307Ch)

Field	Type	Default	Description
Bit 31:8	RO	0x0	Reserved
Bit 7:0	R/W	0x0F	TKIP MIC priority byte AND Mask The Qos control field bit7-0 of the TX/RX Qos data frame is “AND” with this mask to be the priority byte for TKIP MIC calculation.

PHY Control Register

PHY_CSR0: RF/PA configuration register (offset = 3080h)

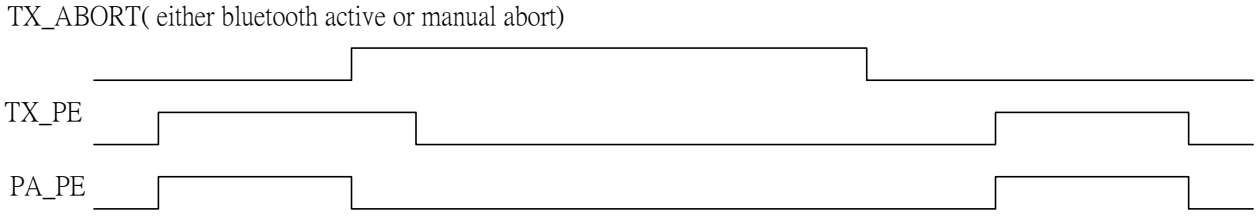
Field	Type	Default	Description
Bit 31:22	RO	0x0	Reserved
Bit 21	R/W	0x0	PA_PE_A polarity 0: Active High 1: Active Low
Bit 20	R/W	0x0	PA_PE_G polarity 0: Active High 1: Active Low
Bit 19	R/W	0x0	PA_PE_A (G) always turn on, 0 : Disable, 1: Enable
Bit 18	R/W	0x0	1: PA_PE_A (G) de-assert with TR_PE switching to RX 0: PA_PE_A (G) de-assert with TR_SW switching to RX
Bit 17	R/W	0x1	1: PA_PE_A pin enable, 0: PA_PE_A always low
Bit 16	R/W	0x1	1: PA_PE_G pin enable, 0: PA_PE_G always low
Bit 15:0	RO	0x0	Reserved

PHY_CSR1: MISC mode configuration register (offset = 3084h)

Field	Type	Default	Description
Bit 31:15	RO	0x0	Reserved
Bit 14	R/W	0x0	0: RX defer after last RXD bit comes in 1: RX defer after io_bb_rx_end asserted Note: Please change both SIFS value to the same one in this mode.
Bit 13	R/W	0x1	0: PAPE stays alive until TX complete in TX abortion 1: Disable PAPE Immediately in TX abortion
Bit 12	R/W	0x0	0: Normal TX mode 1: Manual TX halt (Immediately)
Bit 11	R/W	0x0	0: Disable 1: Enable TX abortion when Bluetooth is active
Bit 10	R/W	0x0	Bluetooth active signal polarity 0: high active 1: low active
Bit 9	R/W	0x1	0: Read BBCR at the beginning of per RX 1: Read BBCR at the end of per RX
Bit 8	R/W	0x1	0: Disable TX retry bit replacement 1: Enable
Bit 7	R/W	0x1	Switch Antenna to TX mode (TRSW =1, TRSWB =0) when LNA low gain (LNA1 = 0, LNA0=1) 0:enable 1:disable
Bit 6	R/W	0x0	1: RF_LE is low when standby 0: RF_LE is high when standby
Bit 5	R/W	0x0	BBP Register R/W mode 1: parallel mode 0: serial mode
Bit 4	R/W	0x1	TXD/RXD mode select 1: 1bit mode 0: 2bit mode

Bit 3	R/W	0x0	OFDM RX equivalent time mode, if the bit set, the processing time is the same at every rate
Bit 2	WC	0x0	Kick one-shot RX in one-shot RX mode Write 1 to kick and self-cleared
Bit 1	R/W	0x0	One-shot RX mode for debugging 1:enable, 0:disable (default)
Bit 0	R/W	0x0	Continuous transmit mode, set the bit if BBP is in continuous TX test mode

- If PHY_CSR.bit11 is enabled, packet transmission will be aborted immediately asbluetooth activation signal is asserted as “active”.
- Manual setting of PHY_CSR1.bit12 to “1” has the same effect to abort TX.
- TX abortion does not influence ACK/CTS TX.



PHY_CSR2: BBP pre-TX CCK (offset = 3088h)

Field	Type	Default	Description
Bit 31	R/W	0x1	1: enable this BBP pre-TX command
Bit 30:24	R/W	0x2	BBP pre-TX register ID for OFDM, default R2
Bit 23:16	R/W	0x18	BBP pre-TX register value for OFDM
Bit 15	R/W	0x1	1: enable this BBP pre-TX command
Bit 14:8	R/W	0x2	BBP pre-TX register ID for CCK, default R2
Bit 7:0	R/W	0x00	BBP pre-TX register value for CCK

- Need not swap I/Q upon transmission in CCK mode. This register is used to match I/Q interface between BBP and RF.

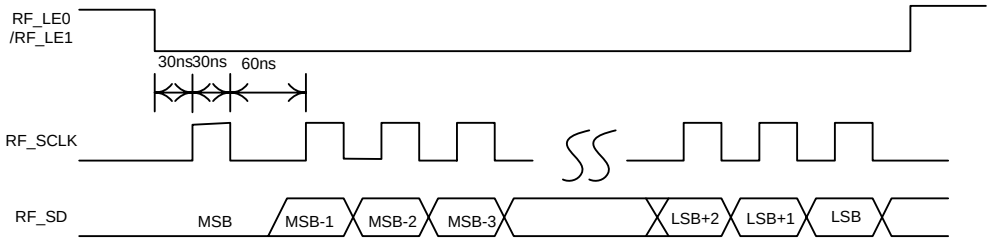
PHY_CSR3: BBP serial control register (offset = 308Ch)

Field	Type	Default	Description
Bit 31:17	RO	0x0	Reserved
Bit 16	R/W	0x0	Write one to kick BBP register read/write Read: Busy
Bit 15	R/W	0x0	Read/write direction, 0: Write, 1: Read
Bit 14:8	R/W	0x0	Select BBP register ID
Bit 7:0	R/W	0x0	BBP data written into or read out from BBP

PHY_CSR4: RF serial control register (offset = 3090h)

Field	Type	Default	Description
Bit 31	R/W	0x0	Write: 1: kick RF register write Read: 1:Busy, 0: Idle
Bit 30	RO	0x0	PLL_LD The current RF PLL_LD
Bit 29	R/W	0x0	RF selection 0:RF_LE0 activate, 1:RF_LE1 activate
Bit 28:24	R/W	0x16	Numbers of bit Default: 22
Bit 23:16	R/W	0x0	RF register ID and content [23:16]
Bit 15:0	R/W	0x0	RF register ID and content [15:0]

- Host should make sure the first bit (MSB in the specified bit number) written to RF is 0 in 1T2R RF chip mode selection.



PHY_CSR5: RX to TX signal switching timing control register (offset = 3094h)

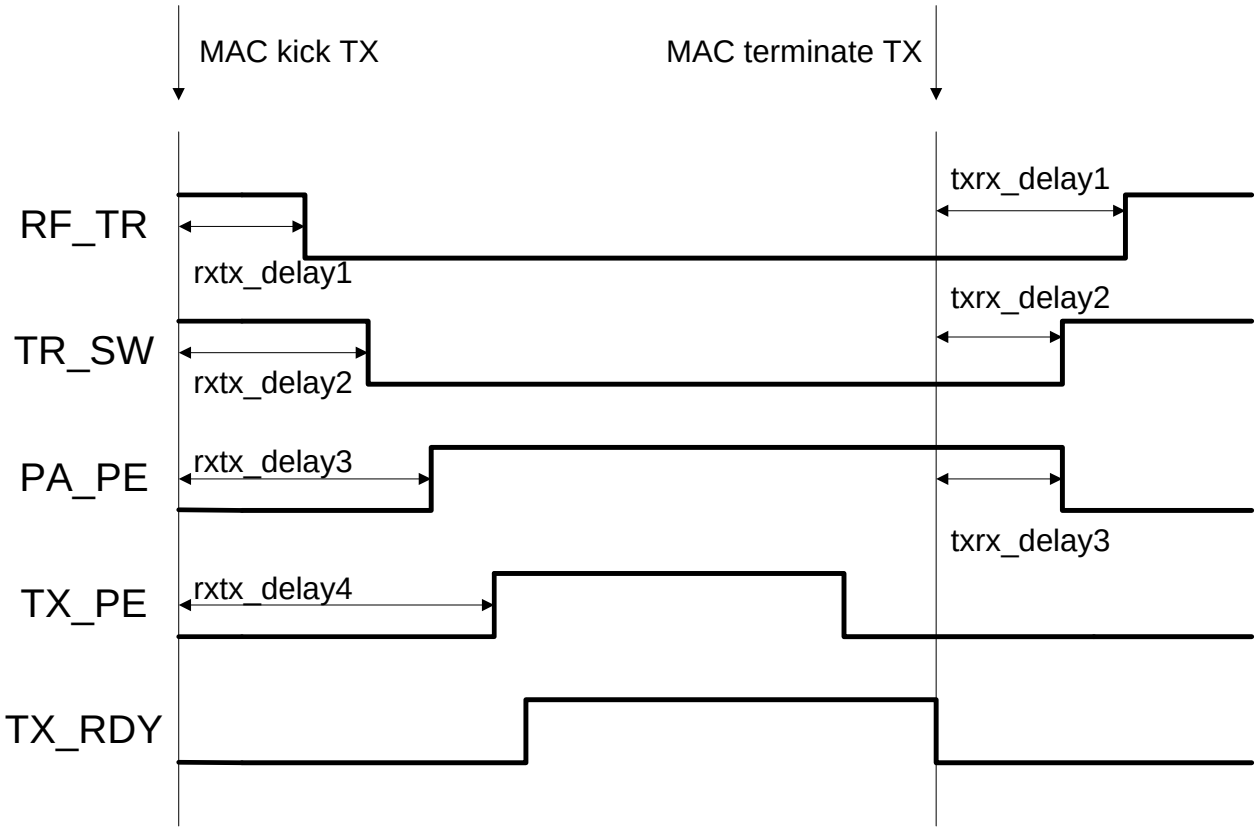
Field	Type	Default	Description
Bit 31:30	RO	0x0	Reserved
Bit 29:24	R/W	0x0	Delay (in unit of 0.25us) from TX kick-off to (RF chip) RF_TR(RF_PE2) enable
Bit 23:22	RO	0x0	Reserved
Bit 21:16	R/W	0x4	Delay (in unit of 0.25us) from TX kick-off to (Antenna) TR_SW enable
Bit 15:14	RO	0x0	Reserved
Bit 13:8	R/W	0x8	Delay (in unit of 0.25us) from TX kick-off to (PA) PA_PE enable
Bit 7:6	RO	0x0	Reserved
Bit 5:0	R/W	0xC	Delay (in unit of 0.25us) from TX kick-off to (BBP) TX_PE enable

PHY_CSR6: TX to RX signal switching timing control register (offset = 3098h)

Field	Type	Default	Description
Bit 31:22	RO	0x0	Reserved
Bit 21:16	R/W	0xC	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (RF chip) RF_TR(RF_PE2) disable
Bit 15:14	RO	0x0	Reserved
Bit 13:8	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (Antenna) TR_SW disable
Bit 7:6	RO	0x0	Reserved
Bit 5:0	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to (PA) PA_PE disable

PHY_CSR7: TX DAC switching timing control register (offset = 309Ch)

Field	Type	Default	Description
Bit 31:14	RO	0x0	Reserved
Bit 13:8	R/W	0x4	Delay (in unit of 0.25us) from TX kick-off to TX DAC enable
Bit 7:6	RO	0x0	Reserved
Bit 5:0	R/W	0x8	Delay (in unit of 0.25us) from (BBP) TX_PE disable to TX DAC disable



SEC Control Register

SEC_CSR0: Shared key table control register (offset = 30A0h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:0	R/W	0x0	Shared key entry valid bit, 1:valid, 0:not valid Bit0 for shared key entry offset 0x000 Bit1 for shared key entry offset 0x020 And so on. Bit15 for shared key entry offset 0x1e0

SEC_CSR1: Shared key table security mode register (key0-7) (offset = 30A4h)

Field	Type	Default	Description
Bit 31	RO	0x0	Reserved
Bit 30:28	R/W	0x0	Security mode for shared key offset @ 0x0e0
Bit 27	RO	0x0	Reserved
Bit 26:24	R/W	0x0	Security mode for shared key offset @ 0x0c0
Bit 23	RO	0x0	Reserved
Bit 22:20	R/W	0x0	Security mode for shared key offset @ 0x0a0
Bit 19	RO	0x0	Reserved
Bit 18:16	R/W	0x0	Security mode for shared key offset @ 0x080
Bit 15	RO	0x0	Reserved
Bit 14:12	R/W	0x0	Security mode for shared key offset @ 0x060
Bit 11	RO	0x0	Reserved
Bit 10:8	R/W	0x0	Security mode for shared key offset @ 0x040
Bit 7	RO	0x0	Reserved
Bit 6:4	R/W	0x0	Security mode for shared key offset @ 0x020
Bit 3	RO	0x0	Reserved
Bit 2:0	R/W	0x0	Security mode for shared key offset @ 0x000

- 0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now)

SEC_CSR2: Pair-wise key entry valid register (offset = 30A8h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0000	64 Pair-wise key entry valid bit , 1:valid, 0:not valid Bit0 for pair-wised key entry offset 0x200 Bit1 for pair-wised key entry offset 0x220 And so on. Bit31 for pair-wised key entry offset 0x5e0

SEC_CSR3: Pair-wise key entry valid register (offset = 30ACh)

Field	Type	Default	Description
Bit 31:0	R/W	0x0000	64 Pair-wise key entry valid bit , 1:valid, 0:not valid Bit0 for pair-wised key entry offset 0x600 Bit1 for pair-wised key entry offset 0x620 And so on. Bit31 for pair-wised key entry offset 0x9e0

SEC_CSR4: Pair-wise key lookup control register (offset = 30B0h)

Field	Type	Default	Description
Bit 31:4	RO	0x0	Reserved

Bit 3:0	R/W	0x0	Pair-wise key table lookup enable According the multiple BSSID mask setting (MAC_CSR5) Case1: when BSSID mask = 2'b11 (one BSSID) Bit0: 1:keytable lookup enable, 0: disable Bit1-3: no effect. Case2: when BSSID mask = 2'b01 or 2'b10 (two BSSID) Bit0: 1:keytable lookup enable for don't care BSSID bit = 1'b0, 0: disable Bit1: 1:keytable lookup enable for don't care BSSID bit = 1'b1, 0: disable Bit2-3: no effect. Case3: when BSSID mask = 2'b00 (four BSSID) Bit0: 1:keytable lookup enable for don't care BSSID bit = 2'b00, 0: disable Bit1: 1:keytable lookup enable for don't care BSSID bit = 2'b01, 0: disable Bit2: 1:keytable lookup enable for don't care BSSID bit = 2'b10, 0: disable Bit3: 1:keytable lookup enable for don't care BSSID bit = 2'b11, 0: disable

- Pair-wise key table lookup shall be performed only when: (unicast-to-me packet) & (BSSID matched) & (Pair-wise key table lookup for the corresponding BSSID is enabled.)

SEC_CSR5: Shared key table security mode register (key8-15) (offset = 30B4h)

Field	Type	Default	Description
Bit 31	RO	0x0	Reserved
Bit 30:28	R/W	0x0	Security mode for shared key offset @ 0x1e0
Bit 27	RO	0x0	Reserved
Bit 26:24	R/W	0x0	Security mode for shared key offset @ 0x1c0
Bit 23	RO	0x0	Reserved
Bit 22:20	R/W	0x0	Security mode for shared key offset @ 0x1a0
Bit 19	RO	0x0	Reserved
Bit 18:16	R/W	0x0	Security mode for shared key offset @ 0x180
Bit 15	RO	0x0	Reserved
Bit 14:12	R/W	0x0	Security mode for shared key offset @ 0x160
Bit 11	RO	0x0	Reserved
Bit 10:8	R/W	0x0	Security mode for shared key offset @ 0x140
Bit 7	RO	0x0	Reserved
Bit 6:4	R/W	0x0	Security mode for shared key offset @ 0x120
Bit 3	RO	0x0	Reserved
Bit 2:0	R/W	0x0	Security mode for shared key offset @ 0x100

- 0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now)

STA Control Register

STA_CSR0: FCS error / RX PLCP error counter (offset = 30C0h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	PLCP error count, cleared by read.
Bit15:0	RC	0x0	FCS error count, cleared by read

STA_CSR1: Long error / CCA false alarm counter (offset = 30C4h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	CCA false alarm count, cleared by read
Bit 15:0	RC	0x0	PHY error count, cleared by read

STA_CSR2: RX FIFO Overflow (offset = 30C8h)

Field	Type	Default	Description
Bit 31:16	RC	0x0	RX Packet buffer overflow error count, cleared by read
Bit 15:0	RC	0x0	MAC RX FIFO overflow count, cleared by read

STA_CSR3: TX beacon counter (offset = 30CCh)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:0	RC	0x0	TX beacon count, cleared by read

STA_CSR4: TX Status Queue (offset = 30D0h)

Field	Type	Default	Description
Bit 31:20	RO	0x0	Reserved
Bit 19:16	RO	0x0	TX successful rate (last TX rate if TX retry fail) 0: 1M 1: 2M 2: 5.5M 3: 11M 4: 6M 5: 9M 6: 12M 7: 18M 8: 24M 9: 36M 10: 48M 11: 54
Bit 15:8	RO	0x0	TX Packet ID (Latched from TX descriptor)
Bit 7:4	RO	0x0	TX retry count
Bit 3:1	RO	0x0	TX result 0: TX OK 1: TX_ZERO_LENGTH 2: TXFIFO_UNDER_RUN 3: reserved 4: TX_PHY_ERROR 5: reserved 6: RETRY_FAIL
Bit 0	RO	0x0	TX status queue valid 0: queue empty, 1: valid

- When ASIC issue “TX_DONE” interrupt to host, host should read CSR_STA4 until the status queue is empty (no longer valid). The TX Packet ID dose NOT include TX beacon packet.

Qos Control Register

QOS_CSR0: TXOP holder address 0 register (offset = 30E0h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	TXOP holder address byte3
Bit 23:16	R/W	0x0	TXOP holder address byte2
Bit 15:8	R/W	0x0	TXOP holder address byte1
Bit 7:0	R/W	0x0	TXOP holder address byte0

QOS_CSR1: TXOP holder address 1 register (offset = 30E4h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:8	R/W	0x0	TXOP holder byte5
Bit 7:0	R/W	0x0	TXOP holder byte4

- It is recommend to fill TXOP holder with all 0s' to park early termination interrupt.

QOS_CSR2: TXOP holder early termination control register (offset = 30E8h)

Field	Type	Default	Description
Bit 31:26	RO	0x0	Reserved
Bit 25	R/W	0x1	0: disable 1: enable TXOP holder early termination check on queue size(QS) value in the QC field(Qos control field). When RX packet is from TXOP holder specified in QOS_CSR0,1 (mactch with Addr2) and QS value is equal to zero, "TXOP holder early termination" interrupt will be issued after CRC check is ok.
Bit 24	R/W	0x1	0: disable 1: enable TXOP holder early termination check on duration field When RX packet is from TXOP holder specified in QOS_CSR0,1 (mactch with Addr2) and duration value is less than or equal to early termination duration threshold specified below, "TXOP holder early termination" interrupt will be issued after CRC check is ok.
Bit 23:16	R/W	0x0	Early termination duration threshold
Bit 15:9	RO	0x0	Reserved
Bit 8	R/W	0x0	0: disable 1: enable TXOP holder early timeout interrupt When this bit is enabled, ASIC will expect CCA while channel listening starts. If ASIC didn't see CCA over the TXOP holder early timeout limit, the "TXOP holder early timeout" interrupt will be issued.
Bit 7:0	R/W	0x0	TXOP holder early timeout limit (unit: 1us)

QOS_CSR3: RX CF-Poll Address1 register0 (offset = 30ECh)

Field	Type	Default	Description
Bit 31:24	RO	0x0	Address1 byte3 of RX CF-Poll Packet
Bit 23:16	RO	0x0	Address1 byte2 of RX CF-Poll Packet
Bit 15:8	RO	0x0	Address1 byte1 of RX CF-Poll Packet
Bit 7:0	RO	0x0	Address1 byte0 of RX CF-Poll Packet

QOS_CSR4: RX CF-Poll Address1 register1 (offset = 30F0h)

Field	Type	Default	Description
Bit 31:17	RO	0x0	Reserved
Bit 16	RO	0x0	1: RX CF-Poll Packet is equal to MAC Address (MAC_CSR2,3)(unicast –to-me) 0: not equal

Bit 15:8	RO	0x0	Address1 byte5 of RX CF-Poll Packet
Bit 7:0	RO	0x0	Address1 byte4 of RX CF-Poll Packet

QOS_CSR5: RX CF-Poll QOS control field register (offset = 30F4h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved
Bit 15:8	RO	0x0	QOS control field byte1 of RX CF-Poll Packet (byte offset =25)
Bit 7:0	RO	0x0	QOS control field byte0 of RX CF-Poll Packet (byte offset =24)

- QOS_CSR3,4,5 is updated right after RX_CF_POLL interrupt.

Security Key Table (Base Address = 0x1000)

■ Security Key Entry Format (32 bytes per key entry)

Offset	Field	Type	Description
0x00	Bit31:0	R/W	Security Key byte3~0
0x04	Bit31:0	R/W	Security Key byte7~4
0x08	Bit31:0	R/W	Security Key byte11~8
0x0C	Bit31:0	R/W	Security Key byte15~12
0x10	Bit31:0	R/W	TX MIC Key byte3~0
0x14	Bit31:0	R/W	TX MIC Key byte7~4
0x18	Bit31:0	R/W	RX MIC Key byte3~0
0x1C	Bit31:0	R/W	RX MIC Key byte7~4

For WEP40, CKIP40: Security Key is valid at byte4~0.
For WEP104, CKIP104: Security Key is valid at byte12~0
For TKIP, AES: Security Key is valid at byte15~0
TX/RX MIC Key is used only for TKIP MIC calculation.

■ Pair-wised Transmitter Address Entry Format (8 bytes per key entry)

Offset	Field	Type	Description
0x00	Bit31:0	R/W	TA byte3~0
0x04	Bit31:0	R/W	Bit [15:0] : TA byte5~4 Bit [18:16] : security mode for the pair 0=no security, 1=WEP40, 2=WEP104, 3=TKIP, 4=AES, 5=CKIP40 6=CKIP104, 7=reserved (no security for now) Bit [31:19] : reserved

■ **Security Key Table Layout (total 3072bytes)**

The security key table is composed of:

1. **16 shared key entries (32x16 bytes)**
2. **32 pair-wise key entries (32x64 bytes, for AP mode)**
3. **32 pair-wise transmitter address entries (8x64 bytes)**

Offset	length	Type	Description
0x000 0x020 0x040 … 0x1e0	32bytes x16	R/W	16 shared key entries According the multiple BSSID mask setting (MAC_CSR5) CASE1. when BSSID mask = 2'b11 (one BSSID): Key entries from 0x000 to 0x060 are treated as shared keys for key id from 0 to 3. CASE2. when BSSID mask = 2'b01or 2'b10 (two BSSID): Key entries from 0x000 to 0x060 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 0 Key entries from 0x080 to 0x0e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 1 CASE3. when BSSID mask = 2'b00 (four BSSID): Key entries from 0x000 to 0x060 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 00 Key entries from 0x080 to 0x0e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 01 Key entries from 0x100 to 0x160 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 10 Key entries from 0x180 to 0x1e0 are treat as shared keys for key id from 0 to 3 if the masked BSSID bit = 11 The key entry format is described above.
0x200 0x220 0x240 …. 0x9e0	32bytes x64	R/W	64 Pair-wised key entries The key entry format is described above.
0xa00 0xa08 0xa10 …. 0xbf8	8bytes x64	R/W	64 Pair-wised transmitter address (TA) entries The mapping of pair-wised TA entries and pair-wised key entries is one-to-one, where TA entry at offset 0x600 maps to offset 0x200 key entry TA entry at offset 0x608 maps to offset 0x220 key entry and so on. TA entry at offset 0x6f8 maps to offset 0x5e0 key entry

PCI Register (Base Address = 0x0000)

PCI register is for host driver use only. Firmware is not able to read or write it. The register clock never stops.

HST_CMD_REG: Host command register (offset = 0008h)

Field	Type	Default	Description
Bit 31:8	RO	0x0	Reserved.

Bit 7	R/W	0x0	Host interrupt request. Asserted by host. Auto cleared.
Bit 6:0	R/W	0x0	Host command.

MCU_CTRL_REG: MCU control register (offset = 000Ch)

Field	Type	Default	Description
Bit 31:4	RO	0x0	Reserved.
Bit 3	R/W	0x0	Stop MCU clock. 1: stop.
Bit 2	RO	0x0	MCU ready.
Bit 1	R/W	0x1	MCU soft reset. 1: reset
Bit 0	R/W	0x0	Program bank select. 1: select program bank.

SOFT_CLKRST_REG: Soft reset and clock enable control register (offset = 0010h)

Field	Type	Default	Description
Bit 31:3	RO	0x0	Reserved.
Bit 2	R/W	0x1	Soft reset PCI module. 0: reset. 1: no use.
Bit 1	R/W	0x1	Host force to enable all MAC module clock. 1: enable all clocks. Will over write any other clock stop setting.
Bit 0	R/W	0x1	Soft reset whole ASIC except PCI module. The EEPROM content will be loaded once more. 0: reset. 1: no use.

MCU_INTSTS_REG: MCU interrupt status register (offset = 0014h)

Field	Type	Default	Description
Bit 31:10	RO	0x0	Reserved.
Bit 9	R/W	0x0	MAC TBCN interrupt. Write 1 to clear.
Bit 8	R/W	0x0	MAC wakeup interrupt. Write 1 to clear.
Bit 7:0	R/W	0x0	MCU interrupt status. Write 1 to clear.

MCU_INTSTS_MSK_REG: MCU interrupt mask register (offset = 0018h)

Field	Type	Default	Description
Bit 31:10	RO	0x0	Reserved.
Bit 9	R/W	0x1	MAC TBCN interrupt mask. 1: mask.
Bit 8	R/W	0x1	MAC wakeup interrupt mask. 1: mask.
Bit 7:0	R/W	0xff	MCU interrupt mask. 1: mask.

PCI_1US_REG: PCI 1uS tick register (offset = 001Ch)

Field	Type	Default	Description
Bit 31:7	RO	0x0	Reserved.
Bit 6	R/W	0x0	1: Enable PCI clock generated 1uS tick.
Bit 5:0	R/W	0x20	1uS dividers parameter when using PCI clock.

Host DMA Register (Base Address = 0x3400)

Both host driver and firmware can read or write DMA registers. However, DMA register is expected for driver use. Firmware should NOT touch it in normal application.

AC0_TXDSCP_BASE: AC0 TX DSCP base address (offset = 3400h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	AC0 TX descriptor base address.

AC1_TXDSCP_BASE: AC1 TX DSCP base address (offset = 3404h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	AC1 TX descriptor base address.

AC2_TXDSCP_BASE: AC2 TX DSCP base address (offset = 3408h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	AC2 TX descriptor base address.

AC3_TXDSCP_BASE: AC3 TX DSCP base address (offset = 340Ch)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	AC3 TX descriptor base address.

MGN_DSCP_BASE: Management TX DSCP base address (offset = 3410h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	Management descriptor base address.

Reserved (offset = 3414h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Reserved.

TXDSCP_TOTAL: Amount of TX DSCP (offset = 3418h)

Field	Type	Default	Description
Bit 31:24	R/W	0x0	AC3 TX descriptor total.
Bit 23:16	R/W	0x0	AC2 TX descriptor total.
Bit 15:8	R/W	0x0	AC1 TX descriptor total.
Bit 7:0	R/W	0x0	AC0 TX descriptor total.

TXDSCP_SIZE: TX DSCP size and Management TXDSCP total (offset = 341Ch)

Field	Type	Default	Description
Bit 31:22	RO	0x0	Reserved.
Bit 21:16	R/W	0x10	TX descriptor size. Unit: DW.
Bit 15:8	RO	0x0	Reserved.
Bit 7:0	R/W	0x0	Management descriptor total.

AIFSN: Aifsn (offset = 3420h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved.
Bit 15:12	R/W	0x0	AIFSN3.
Bit 11:8	R/W	0x0	AIFSN2.
Bit 7:4	R/W	0x0	AIFSN1.
Bit 3:0	R/W	0x0	AIFSN0.

CW_MIN: Cw_min (offset = 3424h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved.
Bit 15:12	R/W	0x0	Cw_min3.
Bit 11:8	R/W	0x0	Cw_min2.
Bit 7:4	R/W	0x0	Cw_min1.
Bit 3:0	R/W	0x0	Cw_min0.

CW_MAX: Cw_max (offset = 3428h)

Field	Type	Default	Description
Bit 31:16	RO	0x0	Reserved.
Bit 15:12	R/W	0x0	Cw_max3.
Bit 11:8	R/W	0x0	Cw_max2.
Bit 7:4	R/W	0x0	Cw_max1.
Bit 3:0	R/W	0x0	Cw_max0.

TX_DMA_DST: TX DMA destination (offset = 342Ch)

Field	Type	Default	Description
Bit 31:10	RO	0x0	Reserved.
Bit 9:8	R/W	0x0	TX DMA destination for management queue. 00: on-chip TX ring0 01: on-chip TX ring1 10: on-chip TX ring2. 11: invalid.
Bit 7:6	R/W	0x2	TX DMA destination for AC3.
Bit 5:4	R/W	0x2	TX DMA destination for AC2.
Bit 3:2	R/W	0x2	TX DMA destination for AC1.
Bit 1:0	R/W	0x2	TX DMA destination for AC0.

KICK_ABR_TX: Kick or abort TX (offset = 3430h)

Field	Type	Default	Description
Bit 31:21	RO	0x0	Reserved.
Bit 20	R/W	0x0	1: Abort management queue. 0: no action. ASIC auto clear this bit after done.
Bit 19	R/W	0x0	1: Abort AC3. 0: no action. ASIC auto clear this bit after done.
Bit 18	R/W	0x0	1: Abort AC2. 0: no action. ASIC auto clear this bit after done.
Bit 17	R/W	0x0	1: Abort AC1. 0: no action. ASIC auto clear this bit after done.
Bit 16	R/W	0x0	1: Abort AC0. 0: no action. ASIC auto clear this bit after done.
Bit 15:5	RO	0x0	Reserved.
Bit 4	R/W	0x0	1: Kick management queue. 0: no action. ASIC auto clear this bit when queue becomes empty or TX abort done.
Bit 3	R/W	0x0	1: Kick AC3. 0: no action. ASIC auto clear this bit when queue becomes empty or TX abort done.
Bit 2	R/W	0x0	1: Kick AC2. 0: no action. ASIC auto clear this bit when queue becomes empty or TX abort done.
Bit 1	R/W	0x0	1: Kick AC1. 0: no action. ASIC auto clear this bit when queue becomes empty or TX abort done.
Bit 0	R/W	0x0	1: Kick AC0. 0: no action. ASIC auto clear this bit when queue becomes empty or TX abort done.

LOAD_TXDSCP: Load TX descriptor base (offset = 3434h)

Field	Type	Default	Description
Bit 31:5	RO	0x0	Reserved.
Bit 4	R/W	0x0	Load management queue base. Write 1 to load. Auto clear.
Bit 3	R/W	0x0	Load AC3 TX descriptor base. Write 1 to load. Auto clear.
Bit 2	R/W	0x0	Load AC2 TX descriptor base. Write 1 to load. Auto clear.
Bit 1	R/W	0x0	Load AC1 TX descriptor base. Write 1 to load. Auto clear.
Bit 0	R/W	0x0	Load AC0 TX descriptor base. Write 1 to load. Auto clear.

AC0_TXDSCP_PTR: Current AC0 TX DSCP address (offset = 3438h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current AC0 TX descriptor address.

AC1_TXDSCP_PTR: Current AC1 TX DSCP address (offset = 343Ch)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current AC1 TX descriptor address.

AC2_TXDSCP_ PTR: Current AC2 TX DSCP address (offset = 3440h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current AC2 TX descriptor address.

AC3_TXDSCP_ PTR: Current AC3 TX DSCP address (offset = 3444h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current AC3 TX descriptor address.

MGN_DSCP_ PTR: Current Management TX DSCP address (offset = 3448h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current Management descriptor address.

Reserved (offset = 344Ch)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Reserved.

RXDSCP_BASE: RX DSCP base address (offset = 3450h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	RX descriptor base address.

RXDSCP_TOTAL_SIZE: Amount of RX DSCP and size (offset = 3454h)

Field	Type	Default	Description
Bit 31:19	RO	0x0	Reserved.
Bit 18:16	R/W	0x4	Total of RX information for write-back by DMA. Excluding own-bit DW. Unit: DW.
Bit 15:14	RO	0x0	Reserved.
Bit 13:8	R/W	0x0	RX descriptor size. Unit: DW.
Bit 7:0	R/W	0x0	Amount of RX descriptor.

RX_CTRL: RX enable and load DSCP (offset = 3458h)

Field	Type	Default	Description
Bit 31:2	RO	0x0	Reserved.
Bit 1	R/W	0x0	Load RX descriptor. Write 1 to load. Auto clear.
Bit 0	R/W	0x0	Enable RX DMA.

RXDSCP_PTR: Current RX DSCP address (offset = 345Ch)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current RX descriptor address.

PCI_CFG: PCI burst configuration (offset = 3460h)

Field	Type	Default	Description
Bit 31:30	RO	0x0	Reserved.
Bit 29:28	R/W	0x3	DMA TX FIFO threshold. 00: 1 DW 01: 2 DW 10: 4 DW 11: 8DW. PCI TX DMA activates only when the free space in TX FIFO is more than the threshold.

Bit 27:26	R/W	0x3	DMA RX FIFO threshold. 00: 1 DW 01: 2 DW 10: 4 DW 11: 8DW. PCI RX DMA activates only when data in RX FIFO is more than the threshold.
Bit 25	R/W	0x1	Disable PCI master DMA after master request ends.
Bit 24	R/W	0x1	Force to disable PCI master DMA immediately.
Bit 23	R/W	0x1	PCI master read command option. 1: Memory read enable. If enable both option, PCI DMA uses memory read multiple only when cache size is greater than the length of one PCI read transaction.
Bit 22	R/W	0x1	PCI master read command option. 1: Memory read multiple enable.
Bit 21:16	R/W	0x0A	Auto check period when run out of RX descriptor. Unit: 32 PCI cycles.
Bit 15	RO	0x0	Reserved.
Bit 14	R/W	0x1	PCI clock run enable.
Bit 13:8	R/W	0x4	PCI RX DMA burst length. Unit: DW.
Bit 7:6	RO	0x0	Reserved.
Bit 5:0	R/W	0x4	PCI TX DMA burst length. Unit: DW.

BUF_FORMAT: buffer data format configuration (offset = 3464h)

Field	Type	Default	Description
Bit 31:14	RO	0x0	Reserved.
Bit 13:8	R/W	0x6	RX data payload offset. Unit: DW.
Bit 7	RO	0x0	Reserved.
Bit 6:0	R/W	0x6	TX data payload offset. Unit: DW.

INT_SRC_REG: Interrupt source register (offset = 3468h)

Field	Type	Default	Description
Bit 31: 22	RO	0x0	Reserved.
Bit 21	R/W	0x0	Manual queue DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 20	R/W	0x0	Management queue DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 19	R/W	0x0	AC3 DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 18	R/W	0x0	AC2 DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 17	R/W	0x0	AC1 DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 16	R/W	0x0	AC0 DMA done interrupt. Issued by DMA. Write 1 to clear.
Bit 15: 6	R/W	0x0	Reserved.
Bit 5	RO	0x0	Reserved.
Bit 4	R/W	0x0	TX abort done interrupt. Write 1 to clear.
Bit 3	RO	0x0	Reserved.
Bit 2	R/W	0x0	Beacon transmission done interrupt. Write 1 to clear.
Bit 1	R/W	0x0	RX done interrupt. Write 1 to clear.
Bit 0	R/W	0x0	MAC TX done interrupt. Write 1 to clear.

INT_MSK_REG: Interrupt mask register (offset = 346Ch)

Field	Type	Default	Description
Bit 31: 22	RO	0x00	Reserved.
Bit 21	R/W	0x1	Manual queue DMA interrupt mask. 1: mask.
Bit 20	R/W	0x1	Management queue DMA interrupt mask. 1: mask.
Bit 19	R/W	0x1	AC3 DMA done interrupt mask. 1: mask.
Bit 18	R/W	0x1	AC2 DMA done interrupt mask. 1: mask.
Bit 17	R/W	0x1	AC1 DMA done interrupt mask. 1: mask.
Bit 16	R/W	0x1	AC0 DMA done interrupt mask. 1: mask.
Bit 15: 8	R/W	0xA	Global interrupt mask period timer. Interrupt won't assert again for a period of time after previous interrupt de-asserted. Unit: 32 PCI cycles. 0xff: period = 0.

Bit 7	R/W	0x0	Enable/disable global interrupt mask period timer. 1: enable. Auto-clear. Enable it before releasing all other mask. Enabling and releasing at the same write is not suggested.
Bit 6	RO	0x0	Reserved.
Bit 5	RO	0x0	Reserved.
Bit 4	R/W	0x1	TX abort done interrupt mask. 1: mask.
Bit 3	RO	0x0	Reserved.
Bit 2	R/W	0x1	Beacon transmission done interrupt mask. 1: mask.
Bit 1	R/W	0x1	RX done interrupt mask. 1: mask.
Bit 0	R/W	0x1	MAC TX done interrupt mask. 1: mask.

EEPROM_REG: EEPROM register (offset = 3470h)

Field	Type	Default	Description
Bit 31:7	RO	0x0	Reserved.
Bit 6	RO	0x0	EEPROM load status. 0: done 1: on loading.
Bit 5	RO	0x0	EEPROM type. 1: 93C46 0: 93C66.
Bit 4	R/W	0x0	EEDO
Bit 3	R/W	0x0	EEDI
Bit 2	R/W	0x0	EECS
Bit 1	R/W	0x0	EESK
Bit 0	R/W	0x0	Reload EEPROM. Write 1 to enable. Self clear when load done.

TXOP01: TXOP0 and TXOP1 (offset = 3474h)

Field	Type	Default	Description
Bit 31:16	R/W	0x0	AC1 TXOP. Unit: 32uS.
Bit 15:0	R/W	0x0	AC0 TXOP. Unit: 32uS.

TXOP23: TXOP2 and TXOP3 (offset = 3478h)

Field	Type	Default	Description
Bit 31:16	R/W	0x0	AC3 TXOP. Unit: 32uS.
Bit 15:0	R/W	0x0	AC2 TXOP. Unit: 32uS.

Reserved (offset = 347Ch)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Reserved.

DMA_STS_REG: DMA status register (offset = 3480h)

Field	Type	Default	Description
Bit 31:30	RO	0x0	Reserved.
Bit 29	R/W	0x0	DMA (PBF interface) RX is blocked over timeout threshold. Write ‘1’ to clear.
Bit 28	R/W	0x0	DMA (PCI interface) RX is idle over timeout threshold. Write ‘1’ to clear.
Bit 27	R/W	0x0	DMA (PBF interface) TX is blocked over timeout threshold. Write ‘1’ to clear.
Bit 26	R/W	0x0	DMA (PCI interface) TX is idle over timeout threshold. Write ‘1’ to clear.
Bit 25:16	R/W	0x040	DMA idle timeout. Unit: 1mS.
Bit 15:10	RO	0x0	Reserved.
Bit 9	RO	0x1	RX DAM in idle.
Bit 8	RO	0x1	TX DAM in idle.
Bit 7:4	RO	0x0	Reserved.
Bit 3	R/W	0x0	PBF RX fifo overflow. Write ‘1’ to clear.
Bit 2	R/W	0x0	PBF RX fifo underrun. Write ‘1’ to clear.

Bit 1	R/W	0x0	PBF TX fifo overflow. Write '1' to clear.
Bit 0	R/W	0x0	PBF TX fifo underrun. Write '1' to clear.

TEST_MODE: Test mode register (offset = 3484h)

Field	Type	Default	Description
Bit 31	RO	0x0	Reserved.
Bit 30	R/W	0x0	Disable radio mode in GPIO.
Bit 29	R/W	0x0	Enable MCU JTAG mode in GPIO.
Bit 28	R/W	0x0	Enable band SW mode in GOPIO.
Bit 27	R/W	0x0	Enable UART mode in GPIO.
Bit 26	R/W	0x0	Enable BT mode in GPIO.
Bit 25:22	R/W	0x0	Reserved.
Bit 21:16	R/W	0x0	GPIO-per-bit ownership. 1: own by mcu.
Bit 15:10	RO	0x0	Reserved.
Bit 9	R/W	0x1	IFS bit option. When set to 1, DMA clears TX descriptor's IFS bit before forwarding to MAC while AC changes.
Bit 8	R/W	0x1	TXOP option. 1: stop TXOP counting when TX buffer is full. 0: count TXOP anyway.
Bit 7	R/W	0x0	Test mode enable.
Bit 6:0	R/W	0x0	Test mode.

UART0_TX: UART0 TX register (offset = 3488h)

Field	Type	Default	Description
Bit 31:15	RO	0x0	Reserved.
Bit 14	RO	0x0	TxBufErr. 1 = TX buffer error. Could be caused by overrun.
Bit 13:9	RO	0x10	TxFrCnt. Free space in TX buffer.
Bit 8	RO	0x0	TxBufFull. 1 = TX buffer full, no more TX byte can be accept.
Bit 7:0	WO	0x0	UART0 TXD

UART0_RX: UART0 RX register (offset = 348Ch)

Field	Type	Default	Description
Bit 31:18	RO	0x0	Reserved.
Bit 17	WO	0x0	Read next RXD byte.
Bit 16	RO	0x0	RxBufErr. 1 = RX buffer error. Could be caused by overrun.
Bit 15	RO	0x0	RxStopErr. 1 = RX stop bit error.
Bit 14	RO	0x0	RxPtyErr. 1 = RX byte parity error.
Bit 13:9	RO	0x0	RxByteCnt. Number of bytes in RX buffer.
Bit 8	RO	0x0	RxDv. 1 = RXD is valid. 0 = RXD is invalid, usually caused by RX buffer empty.
Bit 7:0	RO	0x0	UART0 RXD

UART0_FRAME_CTRL: UART0 frame control register (offset = 3490h)

Field	Type	Default	Description

Bit 31:19	RO	0x0	Reserved.
Bit 18	R/W	0x0	StopBit. Number of stop bits. 0: 1 bit. 1: 2 bits.
Bit 17	R/W	0x0	UartPtyEn. Enable parity bit. 0 = Disable parity bit. No parity bit will be appended to data byte in the disabled mode. 1 = Enable parity bit. The parity could be even or odd, set by parity mode bit.
Bit 16	R/W	0x1	UartPty. Parity mode. 0 = Even parity. 1 = Odd parity. This bit is available only when the parity function is enabled.
Bit 15:0	R/W	0x8E	BRP. Baud rate parameter. The resulting baud rate is: Baud rate = 33MHz/(BRP*2+1) For example, baud rate = 115200, set BRP = 142.

UART0_BF_CTRL: UART0 buffer control register (offset = 3494h)

Field	Type	Default	Description
Bit 31:28	RO	0x0	Reserved.
Bit 27	R/W	0x0	UartEn. UART enable. 1: Enable. 0: disable.
Bit 26	R/W	0x0	RstTx. Soft reset for UART TX module. 1 = Reset. 0 = Normal operation.
Bit 25	R/W	0x0	RstRx. Soft reset for UART RX module. 1 = Reset. 0 = Normal operation.
Bit 24	R/W	0x0	RtsDis. 1 = Force to disable RTS. The RTS will remain low to inform the partner to stop transmission. 0 = Normal operation.
Bit 23	R/W	0x0	CtsDis. 1 = Ignore CTS. The UART performs transmission without checking CTS. 0 = Normal operation.
Bit 22:16	R/W	0x8	IntMskTime, measured in bit time. Interrupt mask time. The interrupt of the same class will not occur again within this period.
Bit 15:8	R/W	0x60	RX idle threshold, measured in bit time. IdleTh is a period of time. Will assert interrupt if SIN remains idle in that period and RX buffer is not empty in that period.
Bit 7:4	R/W	0x8	TX buffer threshold.
Bit 3:0	R/W	0x8	RX buffer threshold.

IO_CTRL: IO control register (offset = 3498h)

Field	Type	Default	Description
Bit 31:5	RO	0x0	Reserved.

Bit 4	R/W	0x1	WLAN active polarity. 1: WLAN_active is active high. 0: WLAN_active is active low.
Bit 3	R/W	0x1	BT active polarity. 1: BT_active is active high. 0: BT_active is active low.
Bit 2	R/W	0x0	RF interface value in power saving mode. 1: set to “0” to all RF interface. 0: normal output.
Bit 1	R/W	0x0	RF interface power saving control. 1: set to Hi-Z. 0: enable output.
Bit 0	R/W	0x0	LED output control in normal operation mode. 1: enable output. 0: LED pad is Hi-Z state.

Reserved (offset = 349Ch)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Reserved.

Reserved (offset = 34A0h)

Field	Type	Default	Description
Bit 31:0	RO	0x1008E	Reserved.

Reserved (offset = 34A4h)

Field	Type	Default	Description
Bit 31:0	RO	0x86088	Reserved.

UART_INT_SRC: UART interrupt source register (offset = 34A8h)

Field	Type	Default	Description
Bit 31:5	RO	0x0	Reserved.
Bit 4	R/W	0x0	UART0 TX buffer error. Write 1 to clear.
Bit 3	R/W	0x0	UART0 RX buffer error. Write 1 to clear.
Bit 2	R/W	0x0	UART0 RX idle threshold interrupt. Write 1 to clear.
Bit 1	R/W	0x0	UART0 TX threshold interrupt. Write 1 to clear.
Bit 0	R/W	0x0	UART0 RX threshold interrupt. Write 1 to clear.

UART_INT_MSK_SRC: UART interrupt mask register (offset = 34ACh)

Field	Type	Default	Description
Bit 31:10	RO	0x0	Reserved.
Bit 9:5	RO	0x1F	Reserved.
Bit 4	R/W	0x1	UART0 TX buffer error interrupt mask. 1: mask.
Bit 3	R/W	0x1	UART0 RX buffer error interrupt mask. 1: mask.
Bit 2	R/W	0x1	UART0 RX idle threshold interrupt mask. 1: mask.
Bit 1	R/W	0x1	UART0 TX threshold interrupt mask. 1: mask.
Bit 0	R/W	0x1	UART0 RX threshold interrupt mask. 1: mask.

PBF_QSTS: PBF queue status (offset = 34B0h)

Field	Type	Default	Description
Bit 31	RO	0x0	Reserved.
Bit 30	RO	0x0	RX queue 1 information FIFO full flag.
Bit 29	RO	0x1	RX queue 1 information FIFO empty flag.
Bit 28	RO	0x0	RX queue 1 information FIFO error flag.
Bit 27	RO	0x0	Reserved.
Bit 26	RO	0x0	TX queue 0 information FIFO full flag.
Bit 25	RO	0x1	TX queue 0 information FIFO empty flag.
Bit 24	RO	0x0	TX queue 0 information FIFO error flag.

Bit 23	RO	0x0	Reserved.
Bit 22	RO	0x0	TX queue 1DMA-to-MCU information FIFO full flag.
Bit 21	RO	0x1	TX queue 1 DMA-to-MCU information FIFO empty flag.
Bit 20	RO	0x0	TX queue 1 DMA-to-MCU information FIFO error flag.
Bit 19	RO	0x0	Reserved.
Bit 18	RO	0x0	TX queue 1 MCU-to-MAC information FIFO full flag.
Bit 17	RO	0x1	TX queue 1 MCU-to-MAC information FIFO empty flag.
Bit 16	RO	0x0	TX queue 1 MCU-to-MAC information FIFO error flag.
Bit 15	RO	0x0	Reserved.
Bit 14	RO	0x0	TX queue 2 DMA-to-MCU information FIFO full flag.
Bit 13	RO	0x1	TX queue 2 DMA-to-MCU information FIFO empty flag.
Bit 12	RO	0x0	TX queue 2 DMA-to-MCU information FIFO error flag.
Bit 11	RO	0x0	Reserved.
Bit 10	RO	0x0	TX queue 2 MCU-to-MAC information FIFO full flag.
Bit 9	RO	0x1	TX queue 2 MCU-to-MAC information FIFO empty flag.
Bit 8	RO	0x0	TX queue 2 MCU-to-MAC information FIFO error flag.
Bit 7	RO	0x0	Reserved.
Bit 6	RO	0x0	RX queue 0 MAC-to-MCU information FIFO full flag.
Bit 5	RO	0x1	RX queue 0 MAC-to-MCU information FIFO empty flag.
Bit 4	RO	0x0	RX queue 0 MAC-to-MCU information FIFO error flag.
Bit 3	RO	0x0	Reserved.
Bit 2	RO	0x0	RX queue 0 MCU-to-DMA information FIFO full flag.
Bit 1	RO	0x1	RX queue 0 MCU-to-DMA information FIFO empty flag.
Bit 0	RO	0x0	RX queue 0 MCU-to-DMA information FIFO error flag.

Firmware DMA Register (Base Address = 0x3400)

Firmware DMA register is dedicated for firmware use. Host driver should NOT touch any of these registers.

FW_TXDSCP_BASE: Firmware TX descriptor base (offset = 34C0h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	TX descriptor base address in firmware manual mode.

FW_TXDSCP_START: Firmware starting TX descriptor (offset = 34C4h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	Starting TX descriptor address in firmware manual mode.

FW_TXDSCP_LAST: Last firmware TX descriptor (offset = 34C8h)

Field	Type	Default	Description
Bit 31:0	R/W	0x0	Last TX descriptor address in firmware manual mode. The next TX descriptor address is FW_TXDSCP_BASE when TX descriptor reaches FW_TXDSCP_LAST.

FW_MAMODE_CTRL: Manual mode control register (offset = 34CCh)

Field	Type	Default	Description
Bit 31:19	RO	0x0	Reserved.
Bit 18	R/W	0x0	1: non-stop TX DMA enable. TX DMA can continuously check TX ring if DMA senses TX ring is empty. This function is available only in manual mode.
Bit 17	R/W	0x0	1: Abort TX in manual mode. 0: no action. ASIC clear kick bit after done.

Bit 16	R/W	0x0	1: Kick TX in manual mode. 0: no action. ASIC clear kick bit when host buffer becomes empty or TX abort done.
Bit 15:12	RO	0x0	Reserved.
Bit 11	RO	0x0	Manual mode is active.
Bit 10	R/W	0x0	Load starting TX descriptor address in manual mode.
Bit 9	R/W	0x0	Force to break DMA burst fetch in manual mode.
Bit 8	R/W	0x0	Manual burst mode enable.
Bit 7:2	R/O	0x0	Reserved.
Bit 1:0	R/W	0x0	DMA destination of on-chip frame buffer in manual mode.

FW_TXDSCP_PTR: Current firmware TX descriptor (offset = 34D0h)

Field	Type	Default	Description
Bit 31:0	RO	0x0	Current TX descriptor address in firmware manual mode. ASIC updates this address at end of fetching a TX frame.

Driver implementation note

Instruction of enabling DMA TX

1. Set TX descriptor base registers:
   (a). AC0_TXDSCP_BASE
   (b). AC1_TXDSCP_BASE
   (c). AC2_TXDSCP_BASE
   (d). AC3_TXDSCP_BASE
   (e). MGN_DSCP_BASE
2. Set TX descriptor configurations:
   (a). TXDSCP_TOTAL
   (b). TXDSCP_SIZE
   (c). AIFSN
   (d). CW_MIN
   (e). CW_MAX
3. Set AC to on-chip buffer destination:
   (a). QMAP
4. Set PCI DMA burst configuration:
   (a). PCI_CFG
5. Load TX descriptor:
   (a). LOAD_TXDSCP
6. Kick TX:
   (a). KICK_TX
7. ASIC clears kick bit when ASIC finds the corresponding queue becomes empty. If all queue are empty, ASIC DMA remains in idle state.

Instruction of disabling DMA TX

1. Driver asserts kick-abort (Reg. KICK_ABR_TX) to disable TX function. DMA module will clear kick bit when a frame transmission (to on-chip buffer) is completely done or the TX DMA is already in idle state.
2. ASIC asserts interrupt once the abort command is done.

Instruction of enabling DMA RX

1. Set RX descriptor base registers:
   (a). RXDSCP_BASE
2. Set RX descriptor configurations:
   (a). RXDSCP_TOTAL_SIZE
3. Set PCI DMA burst configuration:
   (a). PCI_CFG
4. Load RX descriptor
   (a). RX_CTRL
5. Enable RX
   (a). RX_CTRL

Instruction of disabling DMA RX

1. Drive clears RX enable bit (in Reg.0x58) to stop RX DMA.
2. The RX DMA engine will remain in idle state after a frame is completely moved to host memory.

Instruction of initialization LED

1. The LED output is in Hi-Z state after power up. The driver can enable LED output through DMA register IO_CTRL (Reg.3498) bit [0].
2. The LED polarity and blink period are defined at MAC_CORE MAC_CSR14 (in Reg. 0x3038).

Instruction of clock control

1. The clock on/off control in MAC part is turned off if PCI register SOFT_CLKRST_REG (Reg.0010) bit [1] is “1”. Set it to “0” to enable clock on/off function for each MAC sub module.
2. MAC TBCN timer counts down based on a 40MHz clock. While turned off this clock for power saving, need to change the clock base. Set PCI register PCI_1US_REG (Reg.001C) bit [1] to switch the clock base.

Firmware implementation note

Instruction of starting firmware-controlled DMA TX

1. Set TX descriptor address registers:
   (a). FW_TXDSCP_BASE
   (b). FW_TXDSCP_START
   (c). FW_TXDSCP_LAST
2. Set on-chip TX buffer destination:
   (a). FW_MAMODE_CTRL
3. Load starting TX descriptor:
   (a). FW_MAMODE_CTRL
4. Enable manual burst mode:
   (a). FW_MAMODE_CTRL
5. Kick TX
   (a). FW_MAMODE_CTRL

Instruction of stopping firmware-controlled DMA TX

1. Disable TX:
   (a). FW_MAMODE_CTRL
2. Wait firmware TX abort done interrupt:
   (a). FW_INT_SRC_REG
3. Store TX descriptor
   (a). FW_TXDSCP_PTR
4. Disable manual mode:
   (a). FW_MAMODE_CTRL
5. After disable manual mode, TX DMA switches for EDCA queue transmission automatically.

Instruction of implementing HCCA TX in QSTA

1. Driver first gets AP's grant through admission control procedure.
2. When TSPEC stream is ready, driver pushes the frames into HCCA buffer.
3. Firmware starts to send the HCCA frames only when receive QAP CF-Poll. Firmware is in charge of detecting the CF-Poll.
4. When a valid CF-Poll is detected, firmware starts firmware-controlled TX procedure. TXOP burst starts.
5. Firmware needs to maintain TXOP.
6. The termination condition of a TXOP burst:
   (a). TXOP expires
   (b). HCCA ring empty interrupt is asserted.
   (c). Receive a CF-Poll whose DA points to other QSTA.
7. When termination condition occurs, firmware stops firmware-controlled TX procedure. TXOP burst ends.

Instruction of implementing HCCA TX in QAP

1. In QAP application, the HCCA-specific TX tasks are:
   (a). Send CF-Poll to the QSTA that is granted to upload the TSPEC stream.
   (b). Send granted TSPEC download stream to QSTA.
2. A schedule, which specifies the admitted TSPEC stream of a QSTA, is needed. Maintaining schedule is considered as the work between driver and firmware. Detail is not described here.
3. Firmware is expected to control the start and stop of a TX burst according to the schedule.
4. To start a TX burst, firmware uses firmware-controlled TX procedure.
5. The termination procedure is identical to that in HCCA QSTA application.

Instruction of down load 8051 firmware

1. Select on-chip program memory and leave MCU in reset state:
   (a). MCU_CTRL_REG
2. Write program into program memory space, which starts at 0x4000.
3. Close on-chip program memory:
   (a). MCU_CTRL_REG
4. Release MCU reset:
   (a). MCU_CTRL_REG

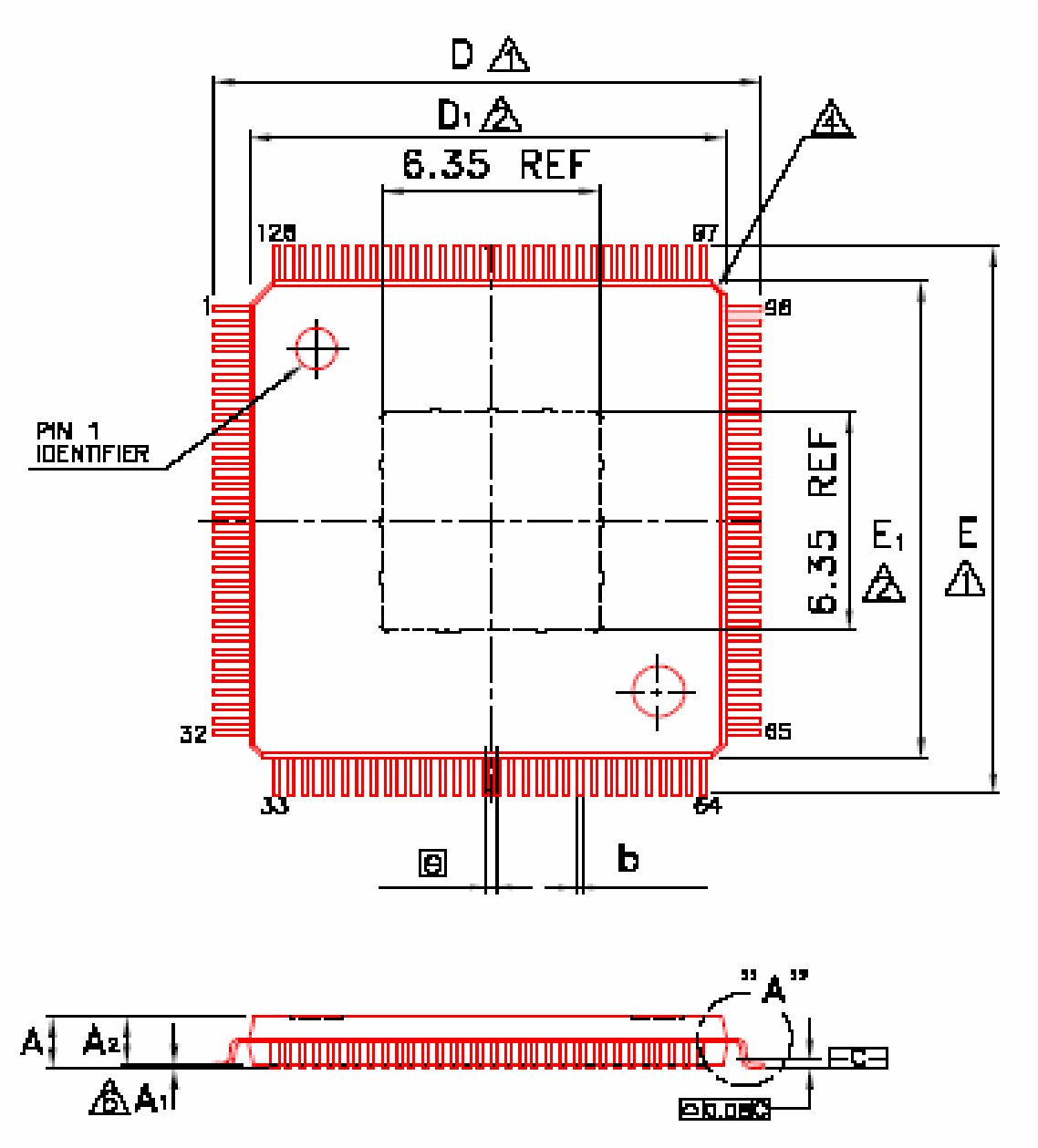
GPIO mode

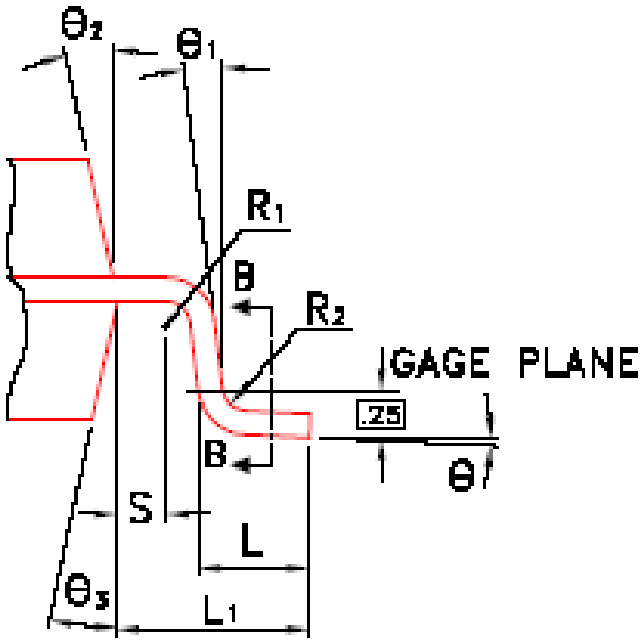
Mode selection						GPIO definition					
MCU GPIO mode	MCU JTAG mode	Radio disable mode	Band SW mode	BT mode	UART mode	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5
111111	X	X	X	X	X	MCU GPIO0	MCU GPIO1	MCU GPIO2	MCU GPIO3	MCU GPIO4	MCU GPIO5/I
000000	1	X	X	X	X	CPU_TDO/O	CPU_TDI/I	CPU_TCK/I	CPU_TMS/I	CPU_TRST/I	GPIO5/I
000000	0	1	1	1	X	Radio disable/O	Band SW_N/O	Band SW_P/O	WL active/O	BT active/I	GPIO5/I
000000	0	0	0	0	1	SOUT/O	RTS_N/O	SIN/I	CTS_N/I	GPIO4	GPIO5/I
000000	0	0	0	0	0	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5/I

The GPIO mode selection is defined in DMA register Reg.0x3484.
GPIO5 is reserved for RADIO_ON. The direction has to set to “input” in MAC_CORE GPIO direction register [5] when this mode is turned on.
Band SW N connects to MAC GPIO register bit [1], Band SW P for GPIO bit [2].

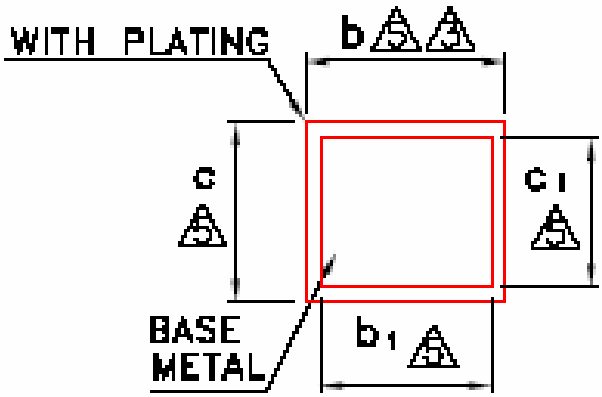
Package Physical Dimension

EPAD-TQFP 128L（14x14x1.2mm）





DETAIL "A"



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.630
D	16.00 BSC			0.630 BSC		
D_1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E_1	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

Revision History

Rev	Date	From	Description
1.0	1/27/05	D. Tung & M. Liu	Initiate the data sheet.
1.1	03/04/05	D. L	1.Add lead-free description on the ordering information 2.The trademarks are added.
2.0	07/04/05	D. Lo	1. Unify the datasheet version 2. Change operating temp. range
3.0	06/28/06	Allie	Unify datasheet version
3.1	12/22/06	Allie Hsieh	Add the disclaimer in the last page
3.3	10/18/07	Mark Liu	Change INTA_N input/output definition from "I" to "O".
3.3	05/14/08	Mark Liu	Update the datasheet. "PCI 2.2 compliant" is added in page one